All communication to and from the system CPU and the parameter cards is in the form of a serial bit stream. [CPU_RXB] and [CPU_TX\] are the receive and transmit lines for the serial data. The system CPU Board controls the sample rate using the signal [TIMETIK\]. [TIMETIK\] is a square wave equal to four times (4X) the AC line frequency (i.e., a typical 60 Hz system produces a [TIMETIK\] frequency of 240 Hz, while a 50 Hz system produces a 200 Hz signal). [TIMETIK\] becomes [TIMETIKI] after passing over the isolation barrier.

5.4.1.3 Connections

All parameter board connections to the ISO Power Supply are made using 30-pin cardedge connectors (J1, J2, J5, J6, J7, and J8). All connectors are clearly labeled within the MPM for easy replacement in the event a parameter board is removed from the MPM.

The ISO Power Supply connects to the MPM Connector Board using cardedge connector J10.

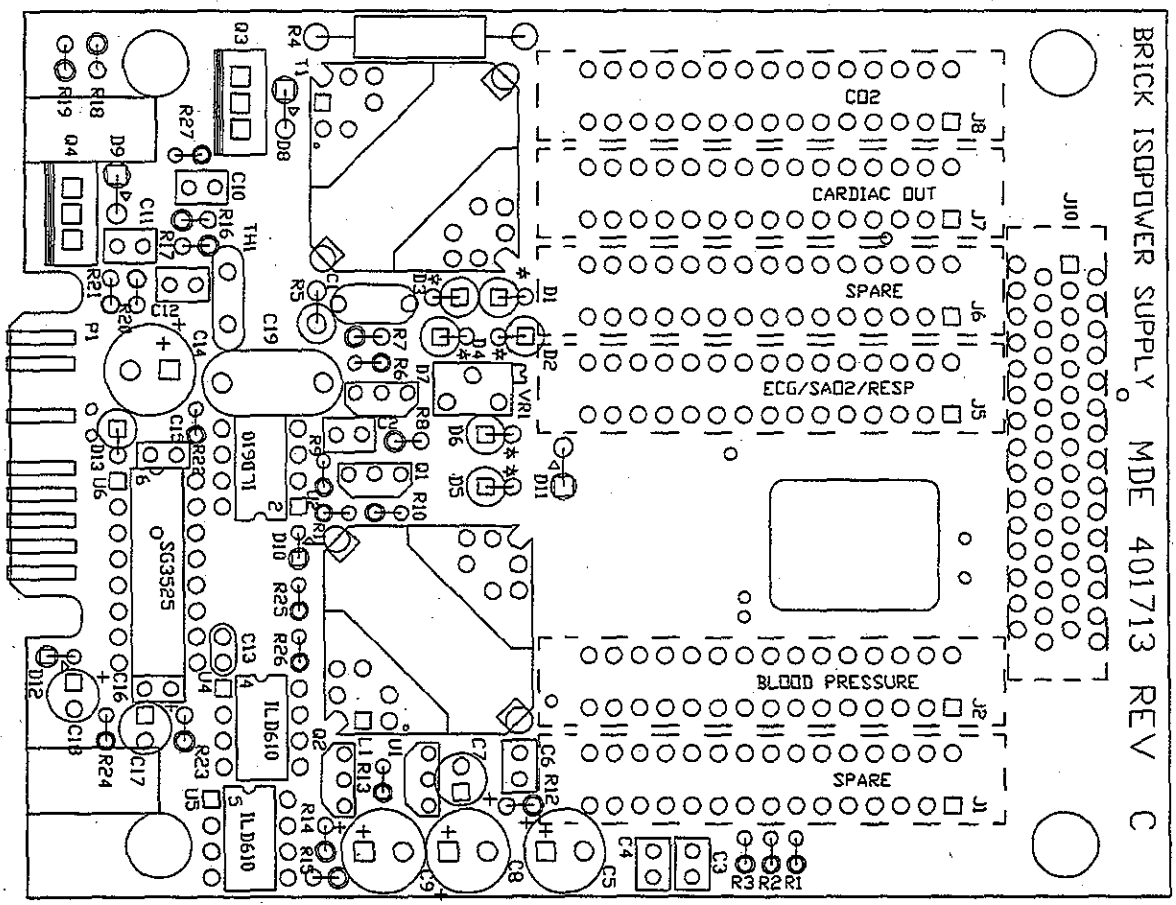


Figure 5-19: MPM ISO Power Supply - Board Layout

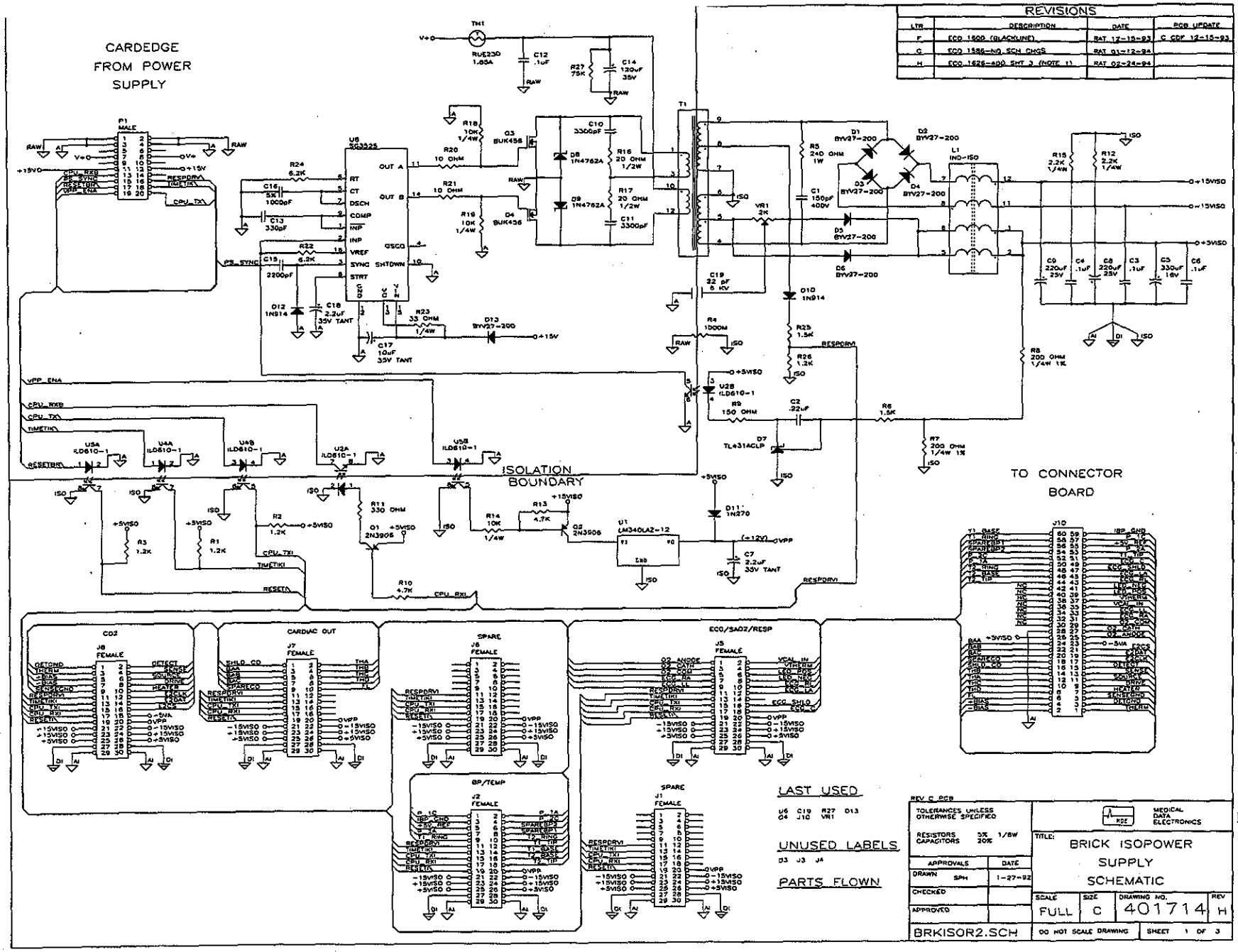


Figure 5-20: MPM ISO Power Supply Schematic 5-21 / 5-22

Table 5-7: Parts Listing, PCBA P/N 401714-0000, MPM ISO Power Supply (1 of 2)

MDE Part Number	Description	Quantity	Reference
352101-0331A	CAP, 330pF,50V,10%,NPO,CER,RAD TAPE & REEL	1	C13
352102-0151A	CAP, 150pF,20%,400VAC,2500V,CS,CER DISC,INT'L APPR	1	C1
352102-0220A	CAP, 22pF,20%,6kV,CER,DISC BULK	1	C19
352200-0127A	CAP, 120uF,35V,20%,LOW ESR,.15/.35,ELECT	1	C14
352201-0337A	CAP, 330UF,16V,ELEC,RAD 3.5mm LEAD SPACE	1	C5
352206-0227A	CAP, 220uF,20%,25V,ELECT,LOW ESR,8x16mm RAD	2	C8, 9
352300-0010A	CAP., 1000pF,5%,MYLAR SORT FROM 352300-0007A	1	C16
352300-0104A	CAP, .1UF,50V,20%,RAD,MYLAR	4	C3, 4, 6, 12
352300-0224A	CAP, .22UF,50V,20%,MYLAR	1	C2
352300-0332A	CAP, .0033UF,50V,20%,RAD,MYLAR,.1 L.S.	2	C10, 11
352301-0222A	CAP, 2200PF,50V,20%,MYLAR	1	C15
352401-0106A	CAP, 10UF,35V,20%,RAD,TANT TAPE & REEL	1	C17
352401-0225A	CAP, 2.2UF,35V,20%,TANT TAPE & REEL	2	C7, 18
354000-0298A	CONN, 30-PIN,F,CARD EDGE	4	J2, 5, 7, 8
354000-0299A	CONN, F,HIGH DENSITY,.050 CNTR,4 ROW	1	J10
364000-0091A	IC, SG 3525	1	U6
364000-0207A	IC, LM78L12ACZ,+ 12V REG TO92	1	U1
364000-0238A	IC, ILD610-1 OPTO ISOLATOR, 2 CHANNEL, DIP 8	3	U2, 4, 5
364000-0240A	IC, TL431ACLP ADJ PRECISION SHUNT DC REG TO-92	1	D7
365000-0008A	SKT, 8-POS,DIP,TIN PLATE,L.P.	3	SU2, 4, 5
365000-0016A	SKT, 16-POS,DIP,TIN PLATE,L.P.	1	SU6
370100-0222A	RES, 2.2K,1/4W,5%,CF TAPE & REEL	2	R12,15
370100-0330A	RES, 33,1/4W,5%,CF TAPE & REEL	1	R23
370101-0100A	RES, 10,1/8W,5%,CF TAPE & REEL	2	R20, 21
370101-0122A	RES, 1.2K,1/8W,5%,CF TAPE & REEL	1	R26
370101-0122A	RES, 1.2K,1/8W,5%,CF TAPE & REEL	3	R1, 2, 3
370101-0151A	RES, 150,1/8W,5%,CF TAPE & REEL	1	R9
370101-0152A	RES, 1.5K,1/8W,5%,CF TAPE & REEL	2	R6, 25
370101-0331A	RES, 330,1/8W,5%,CF TAPE & REEL	1	R11
370101-0472A	RES, 4.7K,1/8W,5%,CF TAPE & REEL	2	R10, 13

Table 5-7: Parts Listing, PCBA P/N 401714-0000, MPM ISO Power Supply (2 of 2)

MDE Part Number	Description	Quantity	Reference
370101-0622A	RES, 6.2K,1/8W,5%,CF TAPE & REEL	2	R22, 24
370101-0753A	RES, 75K,1/8W,5%,CF TAPE & REEL	1	R27
370102-0390A	RES, 39,1/2W,5%,CF TAPE & REEL	2	R16, 17
370200-1002A	RES, 10K,1/4W,1%,MF TAPE & REEL	3	R14, 18, 19
370200-2000A	RES, 200,1/4W,1%,MF TAPE & REEL	2	R7, 8
370201-0241A	RES, 240,5%,1W,M.O. TAPE & REEL	1	R5
370401-0108A	RES, 1000M,1W,5%,2500V	1	R4
374402-0202A	POT, 2K,10-TURN,SIDE ADJ	1	VR1
376000-0011A	XSTR, 2N3906,SIGNAL	2	Q1, 2
376000-0017A	XSTR, BUK456-100A,(OR IRF 540) (TO-220)MOSFET ONLY	2	Q3, 4
378000-0001A	DIO, 1N270 T&R	1	D11
378000-0005A	DIO, 1N914,SIGNAL T&R	2	D10, 12
378000-0041A	DIO, BYV27-200 T&R	7	D1, 2, 3, 4, 5, 6, 13
378000-0061A	DIO, 1N4762A,82V,1W,ZENER TAPE & REEL	2	D8, 9
384000-0192A	THERMISTOR (PCT) RUE185	1	TH1
401713-0000	PCB, BRICK ISOLATION POWER SUPPLY REV C (E1600)	1	-
401905-0000	XFMR, SWITCHING, BRICK PWR SPPLY REV B1 (D551)	1	T1
401906-0000	MULTI-INDCTR,SWTCHNG BRICK/LAB P/S REV A3 (D551)	1	L1

6 ECG/SpO_2/RESP & ECG Processor

6.1 Overview

The ESCORT II provides monitoring capability of ECG, Respiration, and SpO_2 while inhabiting a single slot inside the Multiparameter Module (MPM). The board will include ECG as a minimum, with optional Respiration and SpO_2 when purchased.

ECG signals are developed on the ECG/SpO_2/Resp main board (P/N 401671-0000). The signals are then converted to digital format and routed to the ECG Processor Board (P/N 401675-0000). The digital information is then sent to the ESCORT II's main CPU Board (see Chapter 4 for details).

Respiration is also available on the ECG/SpO_2/Resp main board with the addition of the necessary respiration components and applicable software (P/N 402204-0000).

Pulse Oximetry (SpO_2) monitoring is available with the Nellcor SpO_2 module. This board connects directly to the main ECG/SpO_2/Resp board via the onboard connectors, J2A and J2B.

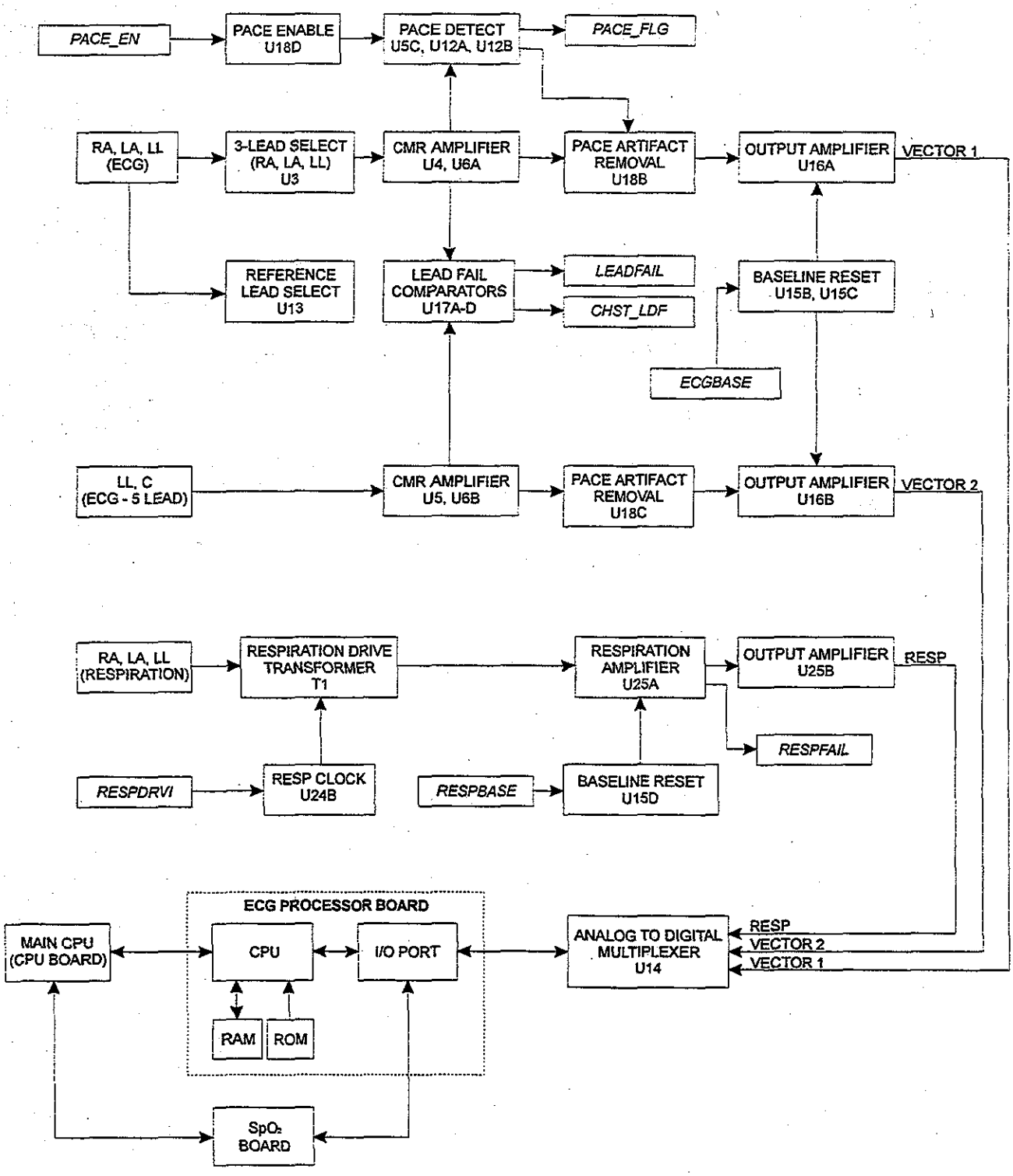


Figure 6-1: ECG/SpO_2/RESP Block Diagram

Note: ***Italicized entries indicate signal names.***

6.2 ECG and Respiration Monitoring

The following sections detail the various circuits utilized on the ECG/SpO_2/Resp Board. Lead select, common mode rejection, amplification, pacer detection, external pacer protection, lead fail, output amplification, respiration, and analog to digital processing are all discussed.

6.2.1 Lead Select Circuit

Lead selection on the ESCORT II is achieved through software via a softkey on the ECG menu. In 3-lead mode, vectors I, II, and III are available. Vector V is available when 5-lead mode is selected. The appropriate lead is selected by the analog switch U3 through the [VSEL0] and [VSEL1] lines, which originate on the ECG Processor Board (see paragraph 6.3). The reference lead is selected by analog switch, U13. Leads LA, RA, LL, and C are buffered by U9A through U9D.

6.2.2 Common Mode Rejection (CMR)

The ECG/SpO_2/Resp Board has circuitry to reject any common mode interference due to outside noise sources (e.g., 60 Hz power line). In 3-lead mode, a differential amplifier (U4) is used for common mode rejection. CMR adjustments are made with VR2. In 5-lead mode, U5 is the differential amplifier and adjustments are made with VR1. See Appendix B for adjustment procedures.

6.2.3 Pacer Pulse Detect Circuit

When the PACE softkey has been set to *ON*, the ESCORT II will reject any pacer artifact and insert a pacer flag into the ECG waveform. The analog ECG signal is available at U4-6 and routed through a band-pass filter comprised of R8, R11, C3, C4, and L1. This filter stage only passes signals with rise times between 16 µs and 20 µs on to U5C, which is used to recognize a pacer pulse. If a fast pulse occurs, it passes through U5C to U12A and U12B. U12A and U12B will determine the polarity of the pulse. If the pulse is positive, U12B becomes active and outputs a 2 ms pulse at U12-7. If the pulse is negative, U12A becomes active and outputs a 2 ms pulse at U12-1. The 2 ms pulse is called [PACE_FLG].

Once a pacer pulse is detected, [PACE_FLG] turns off U18B and U18C blocking the pacer artifact from reaching the ECG output amplifiers. [PACE_FLG] is used by the ECG Processor Board to add a flag to the ECG waveform at the location the pacer was detected.

6.2.4 Lead Fail

In 3-lead mode R15, R3, and R28 (100 MΩ) are used as pull-up resistors. When the ECG inputs are connected to a patient, the voltage at the ECG inputs is approximately 0 VDC with an ECG signal of approximately 1 mV. When a lead becomes disconnected, the pull-up resistor drives the input to +12 volts. Depending on the lead, or combination of leads which disconnect, the output of U4 (pin 6) will either go to +15V or -15V. After passing through U6A, it is routed to the window detector U17C and U17D. If a positive lead fail condition occurs, U17 pin 14 is driven low. If a negative lead fail occurs, U17 pin 13 is driven low. This low level becomes the signal [LEADFAIL], and is sent to the ECG Processor Board.

If the chest lead becomes disconnected, R30 pulls the signal line to +12V. The output of U5 (pin 6) is then driven to either +15V or -15V, and is routed to the window detector U17A and U17B from U6B. The result is the signal [CHST_LDF], which is sent to the ECG Processor Board.

6.2.5 Output Amplifiers

U6A provides the first ECG gain stage (U6B in the chest circuit). The gain of each amplifier is approximately thirty (30). U16A and U16B (VECTOR1 and VECTOR2) are the output amplifiers for the ECG signal. They each produce a gain of approximately 40.

The ECG Processor Board detects any slow baseline shifting, and if necessary, initiates the pulse [ECGBASE] which closes analog switches U15B and U15C. When this switch is activated, a low impedance path is provided on the noninverting inputs of U16A and U16B. This allows the inputs to quickly settle back to their quiescent operating point, and the baseline returns to normal.

6.2.6 Respiration

Respiration is detected by the change in impedance across the patient side of transformer, T1. This is accomplished by injecting a 125 kHz pulse train [RESPDRVI] into Q2, then routing it to a D Flip-Flop (U24B) where it is divided by two producing an operating frequency of 62.5 kHz. This pulse train is then routed into T1. Respiration may then be determined by observing the loading caused by the impedance changes on the patient side. The result is a modulated envelope. The high frequency component is filtered out by R71 and C43. The remaining signal is the Respiration waveform. This signal is then amplified by U25A. If a lead fail condition is present, the [RESPFAIL] signal becomes active and is routed to the ECG Processor Board.

U15D provides the baseline reset pulse into the output amplifier U25B when activated by the signal [RESPBASE]. VR3 is used to zero the output of U25B with no respiration signal applied. The output of U25B is sent to U14, which is an A/D Multiplexer.

6.2.7 Analog-to-Digital Processing

The ECG and Respiration analog signals [VECTOR1], [VECTOR2], and [RESP] are inputs to the Analog to Digital/Multiplexer, U14. U14 is controlled by the ECG Processor via the *DIN* line. Analog information from the inputs are clocked in by the *ACLK* line at 4 MHz. The multiplexed and digitized representation of the analog signals are output at 9600 baud on the *DOUT* line and is sent to the ECG Processor Board. The *SCLK* signal provides the 9600 baud clock.

6.2.8 External Defibrillator and Pacer Protection

The ECG/SpO_2/Resp Board includes a series of opto-isolators which provide electrical protection for the ESCORT II monitor. This protection is supplied to prevent damage to the ECG circuitry when the monitor is connected to an external defibrillator/pacer (Model 20300 only) ***or*** when the monitor is in use and a patient is subjected to defibrillation (Model 20100 and 20300).

The defibrillator provides a signal to the ESCORT II CPU Board during pacer time. This signal is decoded by the ECG Processor Board and is called [EXT_PCBK]. When [EXT_PCBK] is active (low), Q1 turns off creating an open across the source/drain junction and activates [PACE_FLG] through D14. This opens the ground connection from the opto-isolators (U1, U2, U7, U8) internal LEDs. The opto-isolators then open, blocking signals from passing through, as well as providing protection for the ECG input circuit from high current spikes caused by the pacer.

6.2.9 Clock Generator

U10 and U11 derive 4 MHz and 153 kHz clocks. The microprocessor on the ECG Processor Board supplies an 8 MHz clock which is injected into U11A-3. U11A divides the clock frequency by two, producing a 4 MHz clock signal called [ACLK]. [ACLK] is used in two areas, as the clock for the analog to digital/multiplexer (U14) and for the divide by thirteen circuit (U10). U10 divides the 4 MHz down to 306 kHz which is then routed to U11B-11 and divided by two, resulting in a 153 kHz clock. The 153 kHz clock is used as the serial clock (CKA1) on the ECG Processor Board's microprocessor (see paragraph 6.3).

6.2.10 Voltage Regulators

U19, U20, U21, U22, and U23 are three terminal voltage regulators. They provide precision regulation for local use in the analog sections of the ECG/SpO$_2$/Resp Board. R46, R47, and R48 comprise a voltage divider which is used to produce reference voltages of +10 V and -10 V. These reference voltages are used by the comparator U17 to determine the lead fail threshold.

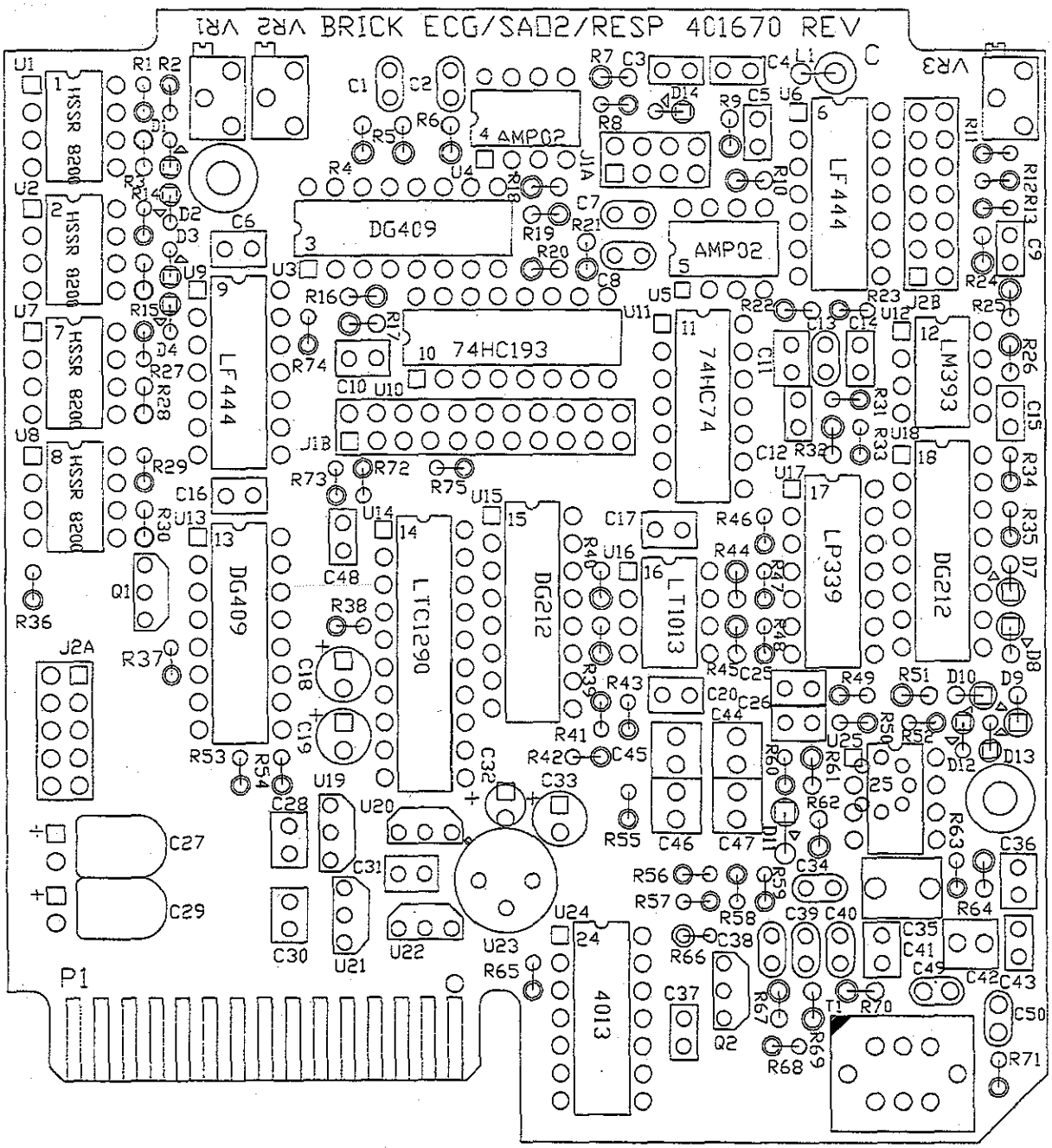


Figure 6-2: ECG Board Layout

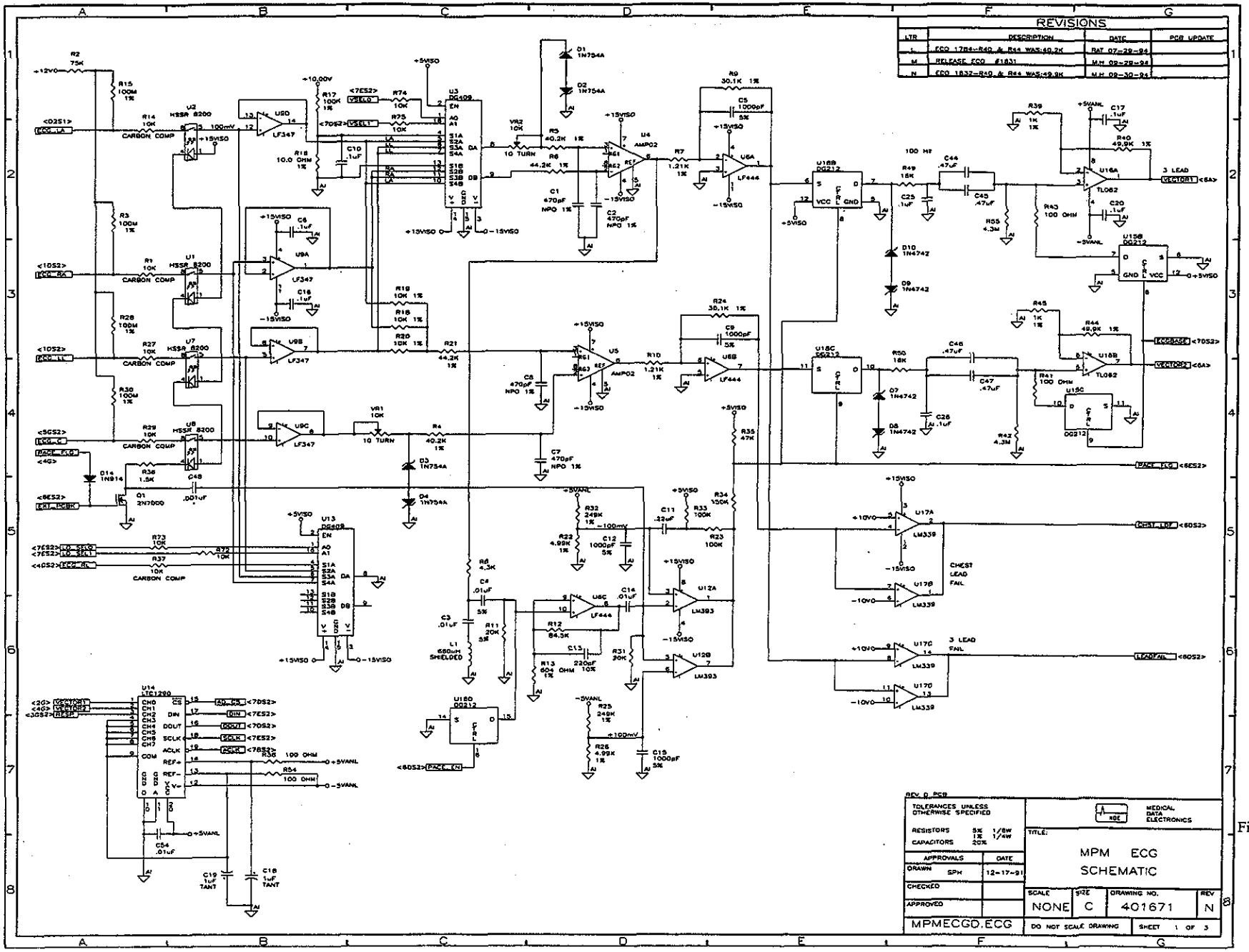


Figure 6-3: ECG/SpO_2/RESP Schematic 6-7 / 6-8

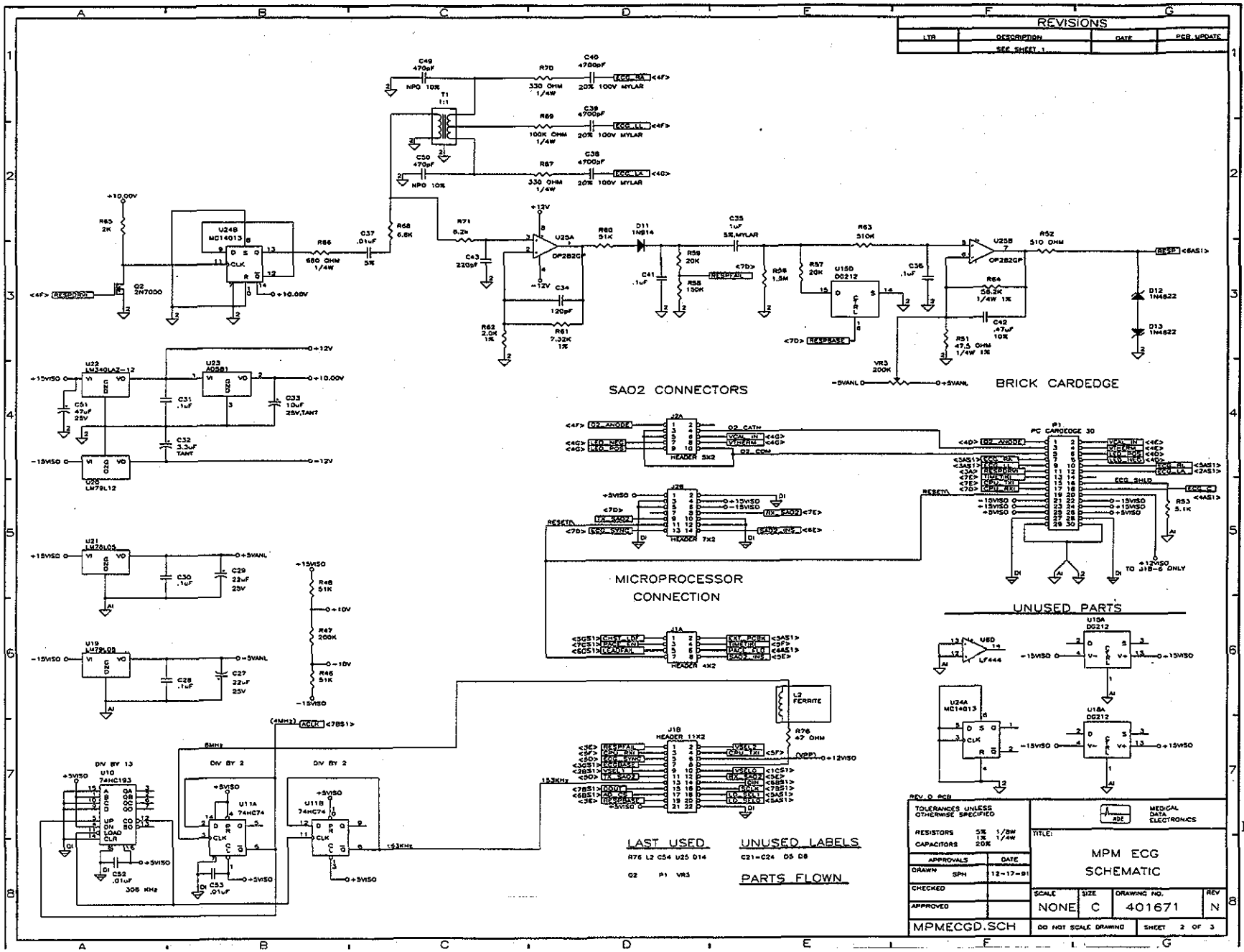


Figure 6-3: ECG/SpO$_2$/RESP Schematic (continued) 6-9 / 6-10

6.3 ECG Processor Board

The ECG Processor Board is the interface between the ECG/SpO_2/Resp Board and the ESCORT II CPU Board. The four main sections are the microprocessor (U2), memory, I/O, and a watchdog timer.

6.3.1 Microprocessor

The microprocessor (U2) is a Z8S180 running at 16 MHz which is determined by crystal X1 (connected to pins 3 and 4). The frequency is divided internally by two, providing an operating frequency of 8 MHz at U2-68. The microprocessor provides I/O control between the ECG/SpO_2/Resp board and the ESCORT II CPU Board. The microprocessor also generates control signals that are used on the ECG/SpO_2/Resp Board.

Synchronization to the ESCORT II system is accomplished by the signal [TIMETIKI] which is equal to four times the line frequency (i.e., a typical 60 Hz system produces a frequency of 240 Hz, while a 50 Hz system produces a 200 Hz signal).

The CPU is the source of the read [RD\] and write [WR\] signals, and the memory enable [ME\] and [IOE\] signals. These signals are used for memory and I/O decoding and routed to U5 and U6.

The signal [TX_SAO2] is used by the CPU for control of the Nellcor SpO_2 OEM board. The SpO_2 patient information is returned to the microprocessor via the signal [RX_SAO2].

Communication to the ECG/SpO_2/Resp Board is accomplished with the signals [DIN] and [DOUT]. Communication to the ESCORT II CPU Board is carried out via the [CPU_RXI] and [CPU_TXI] lines.

The signals [TX_SAO2], [RX_SAO2], [DIN], [DOUT], [CPU_RXI], and [CPU_TXI] are serial communication signals and are clocked at a baud rate of 153 kHz, which is determined by the serial clock on pin 54.

6.3.2 Memory

The memory section of the ECG Processor Board is comprised of EPROM (U1) and RAM (U4). U1 is a 128K Flash EPROM which contains the operating software for the ECG/SpO_2/Resp Board. U4 is a 32Kx8 Static RAM which stores operating parameters and variables while also providing a *scratch pad* for the microprocessor.

6.3.3 I/O Port

I/O Port (U7) is a programmable input/output device (PIO). It provides the main interface between the ECG/SpO_2/Resp and ECG Processor boards.

[VSEL0] and [VSEL1] select the lead configuration for ECG monitoring. [VSEL2] is not used. [LD_SEL0] and [LD_SEL1] determine the reference lead. [ECGBASE] and [RESPBASE] are the ECG and Respiration baseline reset lines. [AD_CS] is the select line for U14, the analog to digital/multiplexer. [EXT_PCBK] controls the external pacer blocking circuit. [PACE_EN] turns the pacer artifact removal and detection circuitry on or off. [SAO2_INS] and [ECG_SYNC] are used for communications with the Nellcor OEM SpO_2 Board. [LDFAIL] and [CHLDFAIL] are indicators of lead fail conditions on the ECG leads. They are the result of the [LEADFAIL] and [CHST_LDF] signals after being filtered by the combination of R9 and C7 for [LEADFAIL] and the combination of R7 and C6 for [CHST_LDF] to remove any high frequency noise.

U3A and U3B are comparators which insure that the [PACE_FLGA] and [RSPFAIL] signals achieve acceptable TTL levels. These signals are derived from the [PACE_FLG] and [RESPFAIL] signals respectively.

6.3.4 Watchdog Timer

The watchdog timer (U8) is used to halt and restart the microprocessor (U2) in the event it becomes unstable or inactive. The watchdog timer is strobed continually by the signal [STROB] which originates at the PIO (U7). If the watchdog is not strobed for more than 150 ms, the [RESET] and [RESET\] lines become active, resetting the microprocessor.

The watchdog will also reset when the main CPU Board issues the signal [RESETI\]. When [RESETI\] goes low, the signals [RESET] and [RESET\] are activated, resetting the microprocessor on the ECG Processor Board.

The watchdog timer also functions as a power monitor. If the supply voltage (+5VISO) falls below 4.5 volts, the [RESET] and [RESET\] signals become active, causing the microprocessor to halt operation until the supply voltage returns to normal.

6.4 NELLCOR® SpO_2 Board (Option 30)

The ESCORT II SpO_2 option provides an automatically calibrated measurement of blood oxygen content as well as deriving a pulse rate. The pulse oximeter utilizes spectrophotometric oximetry and plethysmography principles to obtain these readings.

The SpO_2 finger sensor (NELLCOR Durasensor, MDE P/N E2800-51) utilizes two LEDs as light sources. One emits a red light (approximate wavelength of 660 nm) and the other emits an infrared light (approximate wavelength of 920 nm). A photo detector located on the other end of the finger sensor measures the light that has passed through the sensor point. These values are then used by the pulse oximeter to calculate how much red and infrared light has been absorbed. This information is used to derive the percent of functional hemoglobin that is saturated with oxygen.

Auto-calibration may occur several times in the first minute or two of SpO_2 monitoring, so as to establish a reliable and accurate baseline. Thereafter, the parameter will auto-calibrate about every fifteen (15) minutes. During the calibration sequence, the SpO_2 waveform will appear as a straight line on the ESCORT II screen. Alarms will not be triggered by the calibration sequence.

Communications between the SpO_2 Board and the ECG Processor Board are accomplished with the signals [TX_SAO2] and [RX_SAO2]. The [RESETI\] is used to reset the SpO_2 Board when a system reset is executed. The signal [ECG_SYNC] is provided to support the NELLCOR C-LOCK feature. The [ECG_SYNC] synchronizes the saturation measurements for the best time to perform a SpO_2 reading. If the [ECG_SYNC] is not present, the C-LOCK will not be operational.

The NELLCOR SpO_2 Board is connected to the main ECG/SpO_2/Resp board via connectors, J2A and J2B.

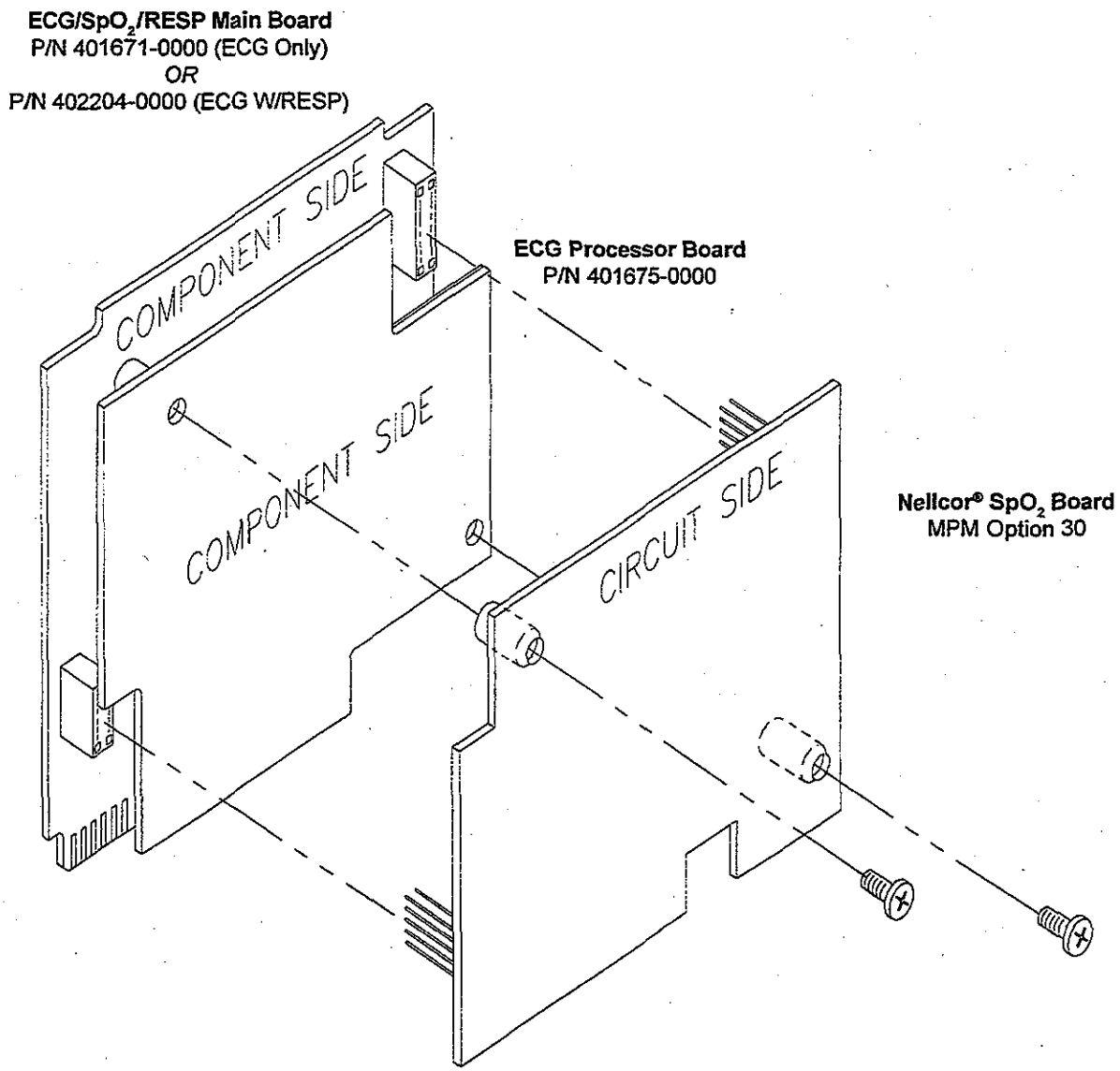


Figure 6-4: ECG/SpO$_2$/Resp Board - PCBA Configuration

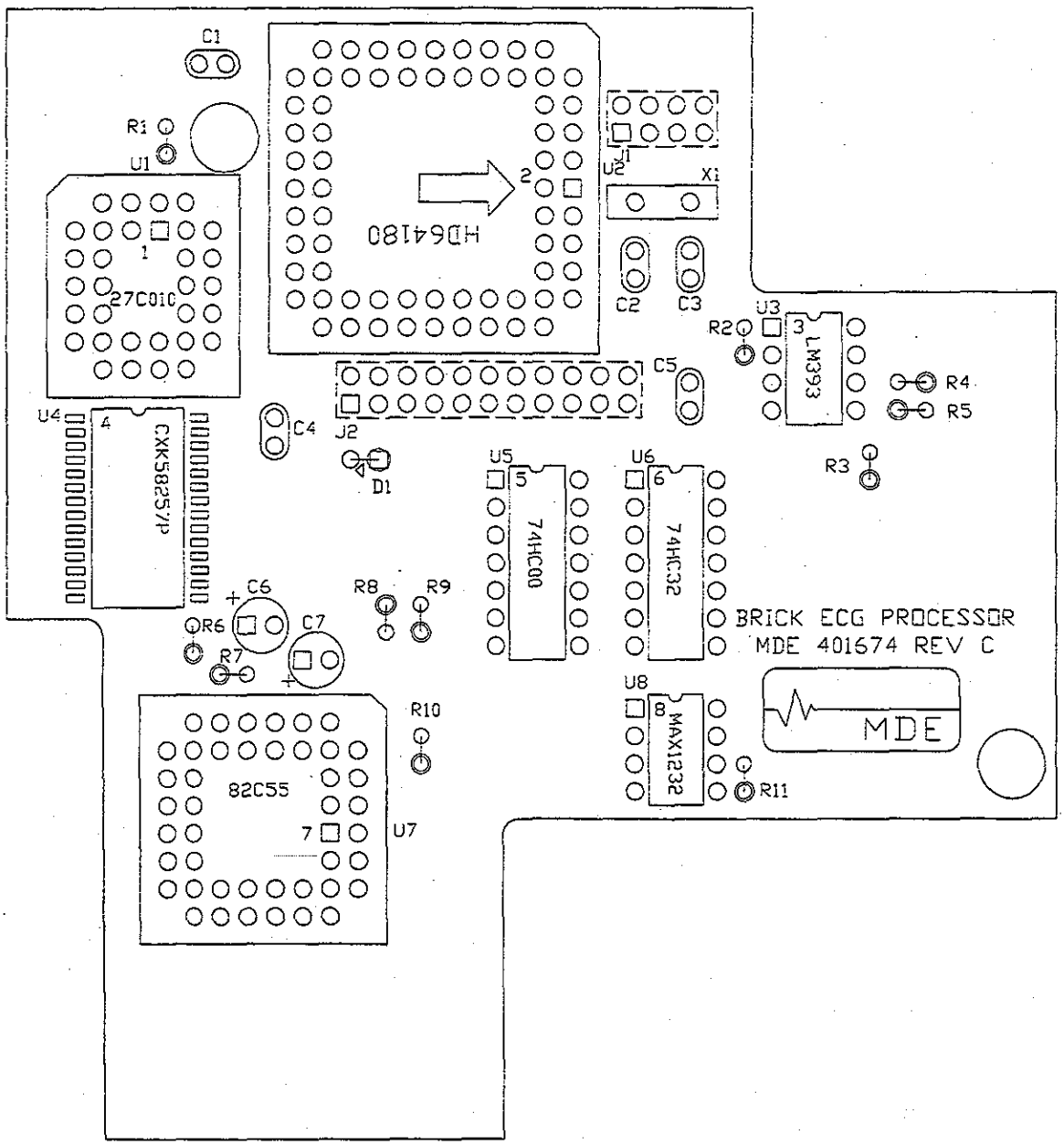


Figure 6-5: ECG Processor Board Layout

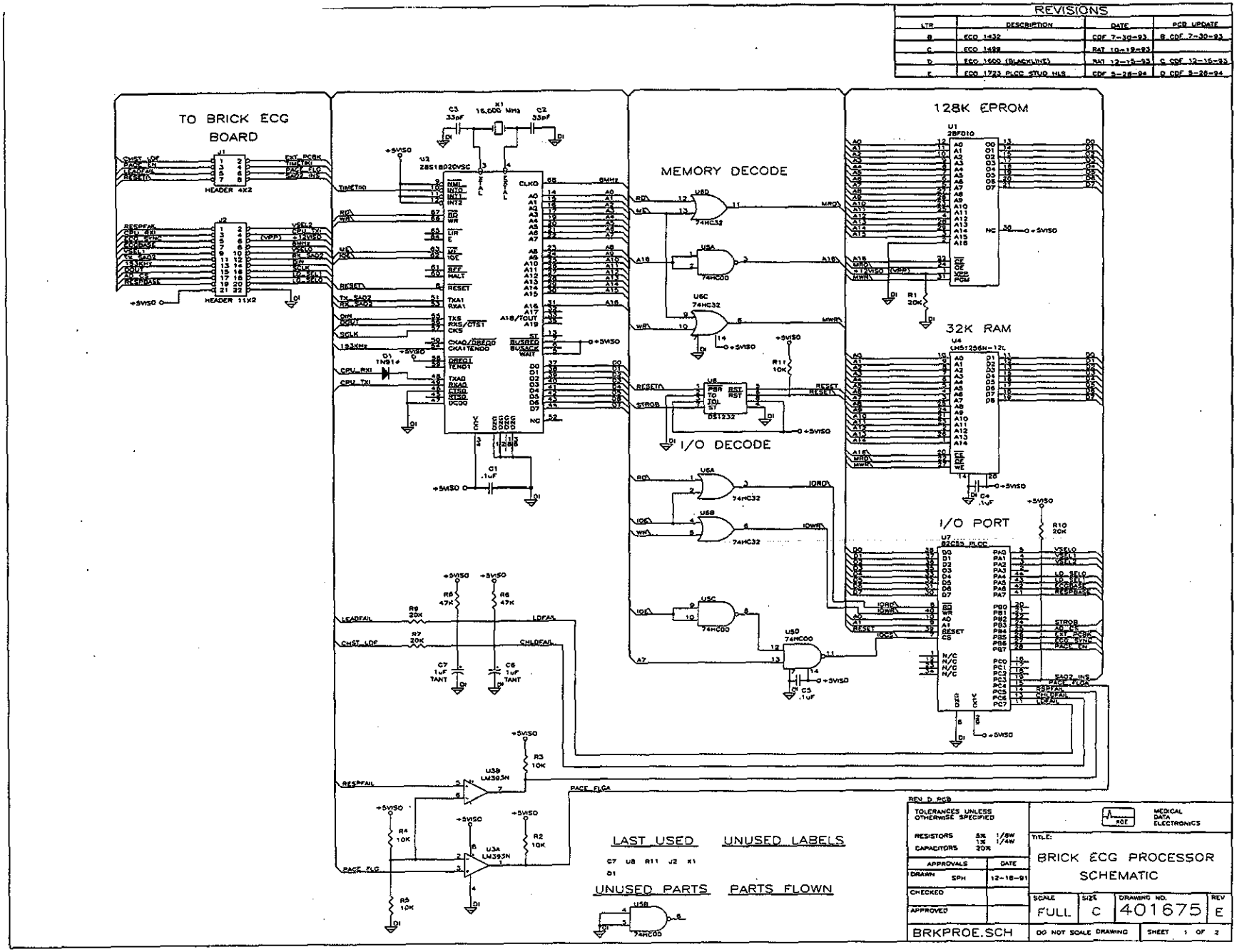


Figure 6-6: ECG Processor Schematic
6-15 / 6-16

Table 6-1: Parts Listing, PCBA P/N 401671-0000, ECG Only Board (1 of 3)

MDE Part Number	Description	Quantity	Reference
352100-0121A	CAP, 120PF,100V,10%,RAD,NPO TAPE & REEL	1	C34
352100-0221A	CAP, 220PF,10%,X7R,.1 L.S. BULK	1	C13
352101-0221A	CAP, 220pF,50V,10%,NPO,CER,RAD TAPE & REEL	1	C43
352101-0471A	CAP, 470pF,10%,50V,RAD,NPO TAPE & REEL	2	C49, 50
352200-0476A	CAP, 47UF,25V,RAD,ELECT 2.5mm LEAD SPACE	1	C51
352300-0007A	CAP, .001UF,10%, MYLAR	1	C48
352300-0008A	CAP, .01UF,5%,MYLAR	1	C14
352300-0008A	CAP, .01UF,5%,MYLAR	3	C3, 4, 37
352300-0010A	CAP., 1000pF,5%,MYLAR SORT FROM 352300-0007A	4	C5, 9, 12, 15
352300-0016A	CAP, .22UF,5%,MYLAR	1	C11
352300-0017A	CAP, .0047UF,10%,MYLAR	3	C38 ,39, 40
352300-0018A	CAP, .47UF,10%,MYLAR	5	C42, 44, 45, 46, 47
352300-0020A	CAP., 1UF,63V,5%,MYLAR	1	C35
352300-0104A	CAP, .1UF,50V,20%,RAD,MYLAR	12	C6 ,10, 16, 17, 20, 25, 26, 28, 30, 31, 36, 41
352400-0105A	CAP,1UF,50V,20%,RAD,TANT, MAX:HT .28; O.D. .16 T&R	2	C18, 19
352400-0106A	CAP, 10UF,25V,20%,RAD,TANT	1	C33
352400-0226A	CAP, 22UF,25V,20%,TANT T & R	2	C27, 29
352400-0335A	CAP, 3.3UF,20V,20%,RAD,TANT TAPE & REEL	1	C32
352600-0044A	CAP, 470pF,1%,50V MIN., NPO	4	C1, 2, 7, 8
354000-0304A	CONN, 72-PIN,F,.1 CTR,D-ROW SOLDER SNAP-AWAY	8	J1A 4x2
354000-0304A	CONN, 72-PIN,F,.1 CTR,D-ROW SOLDER SNAP-AWAY	22	J1B 11x2
354000-0314A	CONN, 10-PIN,F,DUAL ROW,.1 CTR	1	J2A
354000-0315A	CONN, 7-PIN,F,DBL ROW,.1 CTR,.435 HIGH	1	J2B
360500-0118A	STNDOFF, 4-40 x 3/8LG,1/4 DIA ALUM SWAGE	2	2
364000-0008A	IC, DG212CJ	2	U15, 18
364000-0010A	IC, LM339	1	U17
364000-0028A	IC, 74HC74	1	U11
364000-0109A	IC, 78LO5 +5V REG. TO-92 PKG.	1	U21
364000-0110A	IC, 79LO5 ACP -5V REG.	1	U19
364000-0130A	IC, LF347 (SCREENED TO +/- 1.5mV), NATIONAL ONLY	1	U9
364000-0132A	IC, LF444 NATIONAL ONLY	1	U6

Table 6-1: Parts Listing, PCBA P/N 401671-0000, ECG Only Board (2 of 3)

MDE Part Number	Description	Quantity	Reference
364000-0133A	IC, TL062ACP	1	U16
364000-0144A	IC, LM393N,DUAL COMP	1	U12
364000-0175A	IC, HSSR-8200 PHOTOCOUPLER	4	U1, 2, 7, 8
364000-0188A	IC, MC14013B OR 4013B,DIGITAL,DUAL TYPE D FLIPFLOP	1	U24
364000-0207A	IC, LM78L12ACZ,+ 12V REG TO92	1	U22
364000-0208A	IC, LM79L12ACZ NEGATIVE 12V VOLTAGE REG LOW PWR	1	U20
364000-0209A	IC, 74HC193 UP,DOWN COUNTER	1	U10
364000-0210A	IC, LTC1290CCN	1	U14
364000-0211A	IC, AD620BN OP AMP	2	U4, 5
364000-0212A	IC, DG409 ANALOG SWITCH	2	U3, 13
365000-0008A	SKT, 8-POS,DIP,TIN PLATE,L.P.	8	SU1, 2, 4, 5, 7, 8, 12, 16
365000-0014A	SKT, 14-POS,DIP,TIN PLATE,L.P.	5	SU6, 9, 11, 17, 24
365000-0016A	SKT, 16-POS,DIP,TIN PLATE,L.P.	4	SU10, 13, 15, 18
370100-0104A	RES, 100K,1/4W,5%,CF TAPE & REEL	1	R69
370100-0331A	RES, 330,1/4W,5%,CF TAPE & REEL	2	R67, 70
370100-0435A	RES, 4.3M,1/4W,5%,CF TAPE & REEL	2	R42, 55
370100-0681A	RES, 680,1/4W,5%,CF TAPE & REEL	1	R66
370101-0101A	RES, 100,1/8W,5%,CF TAPE & REEL	4	R38, 41, 43, 54
370101-0103A	RES, 10K,1/8W,5%,CF TAPE & REEL	4	R72, 73, 74, 75
370101-0104A	RES, 100K,1/8W,5%,CF TAPE & REEL	2	R23, 33
370101-0152A	RES, 1.5K,1/8W,5%,CF TAPE & REEL	1	R36
370101-0154A	RES, 150K,1/8W,5%,CF TAPE & REEL	2	R34, 58
370101-0155A	RES, 1.5M,1/8W,5%,CF TAPE & REEL	1	R56
370101-0163A	RES, 16K,1/8W,5%,CF TAPE & REEL	2	R49, 50
370101-0202A	RES, 2K,1/8W,5%,CF TAPE & REEL	1	R65
370101-0203A	RES, 20K,1/8W,5%,CF TAPE & REEL	4	R11, 31, 57, 59
370101-0204A	RES, 200K,1/8W,5%,CF TAPE & REEL	1	R47
370101-0432A	RES, 4.3K,1/8W,5%,CF TAPE & REEL	1	R8
370101-0473A	RES, 47K,1/8W,5%,CF TAPE & REEL	1	R35
370101-0511A	RES, 510,1/8W,5%,CF TAPE & REEL	1	R52
370101-0512A	RES, 5.1K,1/8W,5%,CF TAPE & REEL	1	R53
370101-0513A	RES, 51K,1/8W,5%,CF TAPE & REEL	3	R46, 48, 60
370101-0511A	RES, 510,1/8W,5%,CF TAPE & REEL	1	R52

Table 6-1: Parts Listing, PCBA P/N 401671-0000, ECG Only Board (3 of 3)

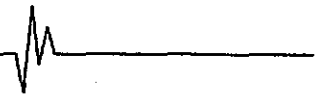
MDE Part Number	Description	Quantity	Reference
370101-0512A	RES, 5.1K,1/8W,5%,CF TAPE & REEL	1	R53
370101-0513A	RES, 51K,1/8W,5%,CF TAPE & REEL	3	R46, 48, 60
370101-0514A	RES, 510K,1/8W,5%,CF TAPE & REEL	1	R63
370101-0622A	RES, 6.2K,1/8W,5%,CF TAPE & REEL	1	R71
370101-0682A	RES, 6.8K,1/8W,5%,CF TAPE & REEL	1	R68
370101-0753A	RES, 75K,1/8W,5%,CF TAPE & REEL	1	R2
370200-0100A	RES, 10,1/4W,1%,MF TAPE & REEL	1	R16
370200-1001A	RES, 1K,1/4W,1%,MF TAPE & REEL	2	R39, 45
370200-1002A	RES, 10K,1/4W,1%,MF TAPE & REEL	3	R18, 19, 20
370200-1003A	RES, 100K,1/4W,1%,MF TAPE & REEL	1	R17
370200-1211A	RES, 1.21K,1/4W,1%,MF TAPE & REEL	2	R7, 10
370200-2001A	RES, 2K,1/4W,1%,MF TAPE & REEL	1	R62
370200-2493A	RES, 249K,1/4W,1%,MF TAPE & REEL	2	R25, 32
370200-3012A	RES, 30.1K,1/4W,1%,MF TAPE & REEL	2	R9, 24
370200-4022A	RES, 40.2K,1/4W,1%,MF TAPE & REEL	2	R40, 44
370200-4422A	RES, 44.2K,1/4,1%,MF TAPE & REEL	2	R6, 21
370200-4750A	RES, 47.5,1/4W,1%,MF TAPE & REEL	1	R51
370200-4991A	RES, 4.99K,1/4W,1%,MF TAPE & REEL	2	R22, 26
370200-5622A	RES, 56.2K,1/4W,1%,MF TAPE & REEL	1	R64
370200-6040A	RES, 604,1/4W,1%,MF TAPE & REEL	1	R13
370202-4022A	RES, 40.2K,1/8W,1%,MF TAPE & REEL	2	R4, 5
370202-7321A	RES, 7.32K,1/8W,1%,MF TAPE & REEL	1	R61
370202-8452A	RES, 84.5K,1/8W,1%,MF TAPE & REEL	1	R12
370403-0103A	RES, 10K,1/4W,5%,CC	5	R1, 14, 27, 29, 37
370500-0107A	RES, 100M,1/4W,5%,M.O. (OR M.G.)	4	R3, 15, 28, 30
374401-0103A	POT, 10K,TRIMM,MULTI-TURN,CERMET FILM (860X)	2	VR1, 2
376000-0019A	XSTR, 2N7000,FET	2	Q1,2
378000-0005A	DIO, 1N914,SIGNAL T&R	2	D11, 14
378000-0009A	DIO, 1N754A,6.8V,ZENER T&R ***MOT ONLY***	4	D1, 2, 3, 4
378000-0020A	DIO, 1N4622,3.9V,10%,ZENER	2	D12, 13
378000-0035A	DIO, 1N4742,12V,+/-5%,ZENER,MOTOROLA	4	D7, 8, 9, 10
382200-0030A	INDCTR, 680uH SHIELDED	1	L1
401670-0000	PCB, SaO2 ECG-B W/RESP BRICK REV C (E1600)	1	-

Table 6-2: Parts Listing, PCBA P/N 402204-0000, ECG with Respiration Board

MDE Part Number	Description	Quantity	Reference
360500-0034A	SPCR, TO-5,PERMA-PAD	1	FOR U23
364000-0205A	IC, OP249 DUAL OP AMP	1	U25
364000-0206A	IC, AD 581 POSITIVE 10V VOLTAGE REGULATOR	1	U23
374402-0204A	POT, 200K,MULTI-TURN,VAR.RES,SIDE-ADJ,CARBON	1	VR3
401671-0000	PCBA, BRICK SpO2 ECG ONLY REV M (E1832)	1	-
401722-0000	XFMR, RESP DRIVE(BRICK) E3B REV A1(D501)	1	T1
402115-0000	SHLD, ECG RESP DRIVE XFMR IN-HSE FAB REV B (E1517)	1	-

Table 6-3: Parts Listing, PCBA P/N 401675-0000, ECG Processor Board

MDE Part Number	Description	Quantity	Reference
352100-0104A	CAP, .1UF,50V,10%,RAD,X7R TAPE & REEL	3	C1, 4, 5
352101-0330A	CAP, 33PF,100V,5%,RAD,NPO TAPE & REEL	2	C2, 3
352400-0105A	CAP,1UF,50V,20%,RAD,TANT, MAX:HT .28; O.D. .16 T&R	2	C6, 7
354000-0106A	CONN, DBL ROW,STRT,SGL PIN,SNAP-AWAY 36-PINS	8	J1 4x2
354000-0106A	CONN, DBL ROW,STRT,SGL PIN,SNAP-AWAY 36-PINS	22	J2 11x2
356000-0026A	XTAL, 16MHZ, LOW PROFILE, .142IN X .425IN	1	X1
364000-0024A	IC, 74HC00	1	U5
364000-0027A	IC, 74HC32	1	U6
364000-0144A	IC, LM393N,DUAL COMP	1	U3
364000-0199A	S*IC, Z80180 8/10MHZ PLCC	1	U2
364000-0213A	IC, WATCHDOG,8-PIN DIP	1	U8
364000-0232A	S*IC, 82C55-PLCC,8 MHZ 200 NANO SEC. OR FASTER SMD	1	U7
364000-0246A	S*IC,51256,SRAM,SMD,32KX8,120NS,SOP28-P-450	1	U4
364000-0278A	S*IC, 1 MEG,UNSECT FLASH PROM PLCC 32,SMD	1	U1 - NEEDS PROGRAM
365000-0044A	S*SKT, 44-PIN,PLCC	1	SU7
365000-0068A	S*SKT, 68-PIN PLCC	1	SU2
365000-0132A	S*SKT, 32-PIN, PLCC	1	SU1
370101-0103A	RES, 10K,1/8W,5%,CF TAPE & REEL	5	R2, 3, 4, 5, 11
370101-0203A	RES, 20K,1/8W,5%,CF TAPE & REEL	4	R1, 7, 9, 10
370101-0473A	RES, 47K,1/8W,5%,CF TAPE & REEL	2	R6, 8
378000-0005A	DIO, 1N914,SIGNAL T&R	1	D1
384000-0182A	TAPE, PRESSURE SENSITIVE MYLAR/POLYESTER	-	AS REQUIRED
401674-0000	PCB, BRICK ECG PROCESSOR REV D (E1723)	1	-



7 BP/TEMP/NIBP Board

7.1 Overview

The BP/TEMP/NIBP Board provides monitoring capability of up to three parameters in eleven different configurations. Available parameters include monitoring of one or two Invasive Blood Pressures (IBP), Temperature (TEMP), and Noninvasive Blood Pressure (NIBP).

Invasive Blood Pressure monitoring is compatible with all **5 µV/V/mmHg** type external pressure transducers. Temperature monitoring utilizes YSI-400 and YSI-700 autosensing circuitry, and is compatible with either type of probe. Noninvasive Blood Pressure monitoring is accomplished using a traditional dual-lumen hose and cuff.

The BP/TEMP/NIBP Board is comprised of five main sections IBP, TEMP, NIBP, NIBP Pneumatics, and Digital Processing.

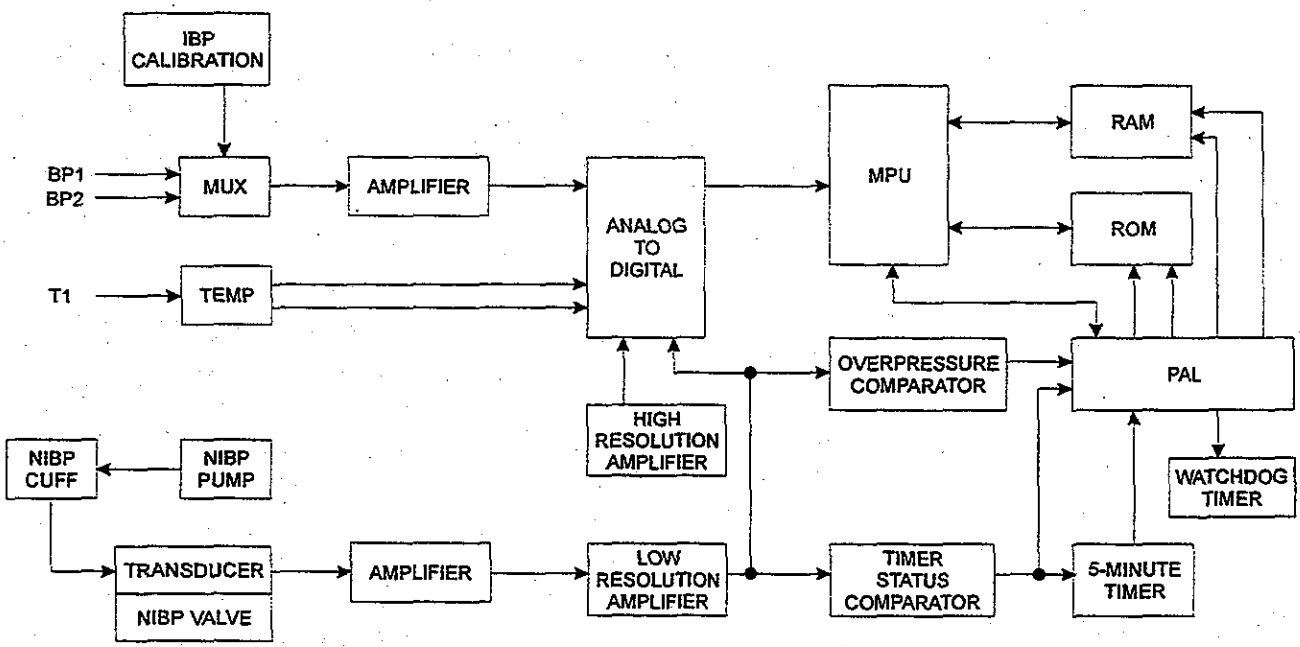


Figure 7-1: BP/TEMP/NIBP Block Diagram

7.2 Invasive Blood Pressure

The BP/TEMP/NIBP Board provides monitoring capability of one or two invasive blood pressures. Excitation voltage (+5 V) to the external IBP transducers is supplied via [+5V_REF], which is a precision reference generated locally on the BP/TEMP/NIBP Board (see paragraph 7.6). The transducer output from IBP Channel 1 enters the circuit via the signals [P_1C] and [P_1A]. IBP Channel 2 utilizes the signals [P_2C] and [P_2A]. Transducer ground is referenced to analog ground using [IBP_GND] for both channels.

The output from the IBP transducer passes through low resistance, series resistors R45 and R46 (IBP Channel 1). R47 and R48 provide the low resistance path for IBP Channel 2. Input filtering is accomplished using C16, C17, and C21 for Channel 1. C19, C20, and C22 provide the filtering for Channel 2. The transducer signals are then routed to a four-channel multiplexer (U9). The multiplexer is controlled by the signals [MUXA] and [MUXB] on pins 10 and 9 respectively.

IBP Channel 1 is connected to multiplexer inputs 0X and 0Y. IBP Channel 2 is connected to inputs 3X and 3Y. The X and Y inputs of the third channel (2X, 2Y) are tied together. When the third channel is selected, the internal resistance of the multiplexer is applied across the inputs of the instrumentation amplifier (U8). The output of the amplifier then establishes the zero reference, *MUX Ground*. The fourth channel of the multiplexer (1X, 1Y) is connected to a voltage divider which is used for IBP calibration. The voltage divider is comprised of precision resistors R8, R9, R10, R14, R15, and variable resistor VR1. The voltage divider supplies approximately 1 to 2 mV which simulates a pressure reading of 100 mmHg. This is used for gain correction and establishes *MUX Reference*. When no IBP transducer is connected, the output of the instrumentation amplifier is driven to +5 V by R36 and R37.

The multiplexed signals are sampled at two different rates; *MUX Ground* and *MUX Reference* are sampled at 30 Hz, and the IBP channels are sampled at 120 Hz. All signals pass through the instrumentation amplifier (U8), which supplies a gain of 414. The resulting data string is the signal [BP], and includes *MUX Ground*, *MUX Reference* and the IBP data. [BP] is then sent to the analog to digital converter (U10-1).

7.3 Temperature

Temperature monitoring on the BP/TEMP/NIBP Board supports both YSI-400 and YSI-700 type temperature probes. Temperatures between 20° C and 50° C may be accurately measured in 0.1° C increments. When no probe is present, 0° C is sent to the ESCORT II CPU Board and dashes are displayed on the screen in place of temperature digits. Temperature readings that are out of range (i.e., below 20° C *or* above 50° C) will also display dashes on the ESCORT II screen.

The probe ring voltage determines the presence of a probe and the probe type. A ring voltage of 20 mV or less indicates that a YSI-400 type probe is connected. A ring voltage higher than 20 mV indicates a YSI-700 type probe. [T1_RING] represents the probe ring voltage and is pulled to +5 V by R49 when no probe is connected. [T1_RING] is then sent to an analog to digital converter (U10-2).

Temperature measurements are derived from the probe tip voltage which is measured with the signal [T1_TIP]. [CAL_SW] is a control signal from Latched Driver (U7) and is routed to Q1. [CAL_SW] is always low, and Q1 is always off. [T1_TIP] is connected to +5 V through precision resistor R51. Another precision resistor, R43, forms a voltage divider with R51 to enable accurate temperature measurements. [T1_TIP] is routed to the analog to digital converter (U10-3). The tip voltage is sampled at a rate of 30 Hz. Every sixteen (16) samples are averaged and compared to a table in the temperature software which spans the temperature range.

[T1_BASE] is driven by Q3 with [T1EXC_SW]. [T1EXC_SW] is an output of Latched Driver (U7) and is always at +5 V. Q3 is always on, which keeps [T1_BASE] at ground.

7.4 Noninvasive Blood Pressure (NIBP)

NIBP uses a pressure transducer referenced to +5 V with an output of 50 μV/mmHg. The output of the transducer is connected to the inputs of an instrumentation amplifier (U2). This is the same type of amplifier used in the IBP circuit. The amplifier is referenced to -1.2 V via the voltage divider formed by R17 and zener diode D1. The gain is adjusted with VR2. When correctly referenced and adjusted, the output of U2 should be -1.24 VDC when zero pressure is applied to the transducer. The nominal gain of the amplifier is approximately 250. The NIBP offset is provided by the potentiometer VR3.

The output of U2 is connected through R22 and R5 to the high and low resolution channels of the circuit. The high resolution channel consists of a low gain amplifier (U3D) with a gain of about 50. A digital-to-analog converter (DAC), U4, is used as a level control loop to center the output pulse waveform at a fixed position in a 0 V to 5 V window. The low resolution channel is made up of a unity gain amplifier (U3C). The total gain output of the high resolution channel is approximately 12,500. The total gain of the low resolution channel is about 250.

The high resolution channel is used to detect the pulse waveform and pulse amplitude. In ADULT mode, the cuff is deflated in 8 mmHg steps. After each step, the DAC level control loop recenters the pulse waveform in the 0 V to 5 V window, essentially mapping each 8 mmHg step into the window. The resolution of this channel is about 625 mV/mmHg or about 512 counts/mmHg at the DAC. In PED and NEO modes, the cuff is also deflated in 8 mmHg steps. However, when the cuff pressure goes below 28 mmHg, the cuff is deflated in 4 mmHg steps.

The low resolution channel provides an output voltage which corresponds to the actual cuff pressure. The signal from the high gain amplifier (U2) is connected through the unity gain amplifier (U3C) to output a signal between 0 V and 5 V. The resolution of this channel is about 12.5 mV/mmHg or 10.2 counts/mmHg. The output of the low resolution channel is also connected to the input of the overpressure and timer control comparators (U3A and U3B).

The comparators U3A and U3B monitor the hardware safety features of the NIBP parameter. U3A is referenced to a voltage equivalent to 15 mmHg. Whenever the input signal from the low resolution channel is equal to or greater than the reference, the 5-Minute Timer Circuit (U5) is started. The [STAT5MIN] flag is set at the Programmable Array Logic (PAL) Decoder (U14) when the 5-Minute Timer is started. The [TIME_OUT] flag is set when the timer times out, and the PAL sends the [FAIL_INT] to the microprocessor unit (MPU), U16. The 5-Minute Timer is reset when the cuff pressure falls below 15 mmHg through D9 and D10. U3B is referenced to the [ADT/NEO\] select line to sense for overpressure conditions. When the [ADT/NEO\] signal is high, the ESCORT II is in either ADULT or PED mode; when low, it is in the NEO mode. The ADULT mode references pressures from 265 to 275 mmHg. The NEO reference is equal to 160 mmHg. The [FAIL_OP] flag is set at the PAL when the overpressure limit is violated, and immediately it sends the [FAIL_INT] signal to the MPU.

7.4.1 NIBP Pneumatics

The NIBP pneumatics section includes the Pneumatics Assembly (P/N 401966-0000) and the Pump Assembly (P/N 401965-0000). The two assemblies are controlled by the NIBP circuitry to inflate and vent the NIBP cuff. The NIBP pneumatics section is detailed in Figure 7-2.

When the NIBP **START** softkey is pressed, power (approximately 12 VDC) is applied to the pump (P2) and to the cuff valve (VAL1), allowing the cuff to inflate through the bottom NIBP hose connector. A check valve is included in the pneumatics assembly and is used to maintain the cuff pressure after inflation.

Cuff pressure is sensed by the pressure transducer (U1) which is installed in the NIBP manifold adjacent to the top NIBP hose connector.

Overpressure protection is provided by the pump's relief valve which will open at 330 mmHg and vent the system.

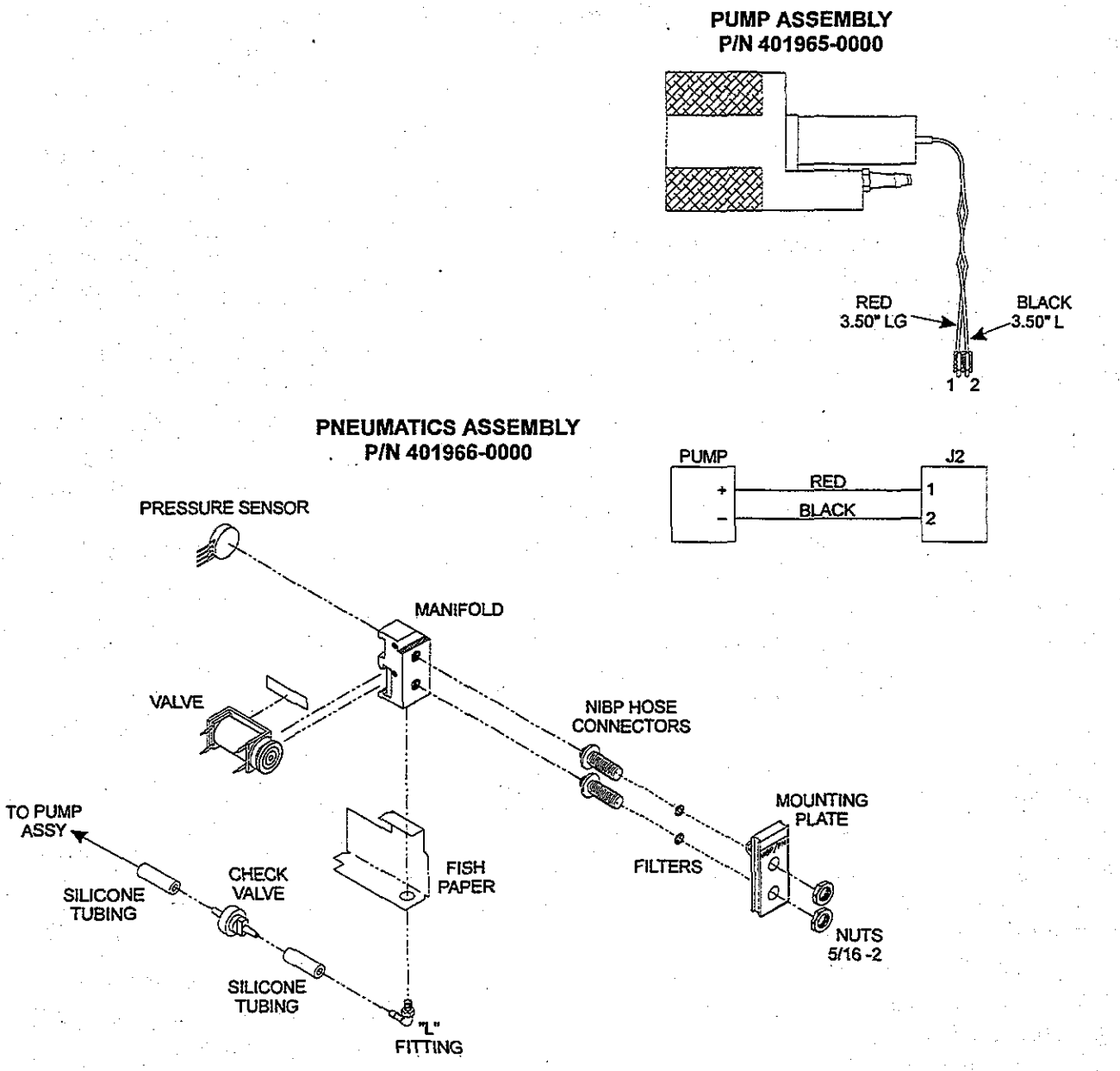


Figure 7-2: NIBP Pneumatics

7.5 Digital Processing

The BP/TEMP/NIBP digital section consists of a microprocessor (U16), PAL decoder, watchdog timer, memory, latched drivers (U7, U8), and an analog-to-digital converter.

7.5.1 Microprocessor

The microprocessor (U16) is a Z8S180 running at 16 MHz which is determined by crystal X1 (connected to pins 3 and 4). The frequency is divided internally by two, producing an operating frequency [ACLK] of 8 MHz at U16-68, and as [SCLK] at U16-57. The signal [TIMETIKI] maintains synchronization in the Multiparameter Module (MPM) and is shared by all parameter boards within the MPM.

[TIMETIKI] is the isolated version of [TIMETIC] whose frequency is equal to four times (4X) the AC line frequency. A typical 60 Hz system produces a [TIMETIC] frequency of 240 Hz while a 50 Hz system produces a [TIMETIC] frequency of 200 Hz. [TIMETIKI] is connected to the microprocessor INT1 line (U16-11).

7.5.2 PAL Decoder

The BP/TEMP/NIBP parameter board uses a Programmable Array Logic (PAL) Decoder (U14) to process signals from the microprocessor and the NIBP circuitry. The PAL receives the [TIME_OUT], [FAIL_OP], and [STAT5MIN] signals directly from the NIBP circuitry. It outputs [FAILINT\] to the microprocessor INT0 (U16-10) when either [TIME_OUT] or [FAIL_OP] is received from NIBP. The PAL controls the output enable on the latch drivers (U6 and U7) through the OE line (U6-14 and U7-14) with the [OE5800\] signal, which is also sent to the high current driver (U19A) for the NIBP pump and valve. At the same time, the PAL also sends the [LD5800] signal for strobing the latch drivers. In addition, the PAL controls the onboard memories with [RAM_WR\], [RAM_OE\], [FLSH_WR\] and [FLSH_OE\]. The PAL strobes the Watchdog Timer with [WD_ST\] every 1.2 seconds, which indicates that the board is operating correctly and it does not need to be reset. The PAL is involved in taking NIBP readings by adjusting the high resolution channel with the signal [DAC_LD\] to the DAC (U4).

7.5.3 Watchdog Timer

The Watchdog Timer circuit (WD) is strobed by the [WD_ST\] signal line from the PAL Decoder (U4) every 1.2 seconds. If the [WD_ST\] signal does not occur, then the Watchdog Timer will reset the microprocessor, and the latch drivers with signals [WD_RST\] and [WD_RST]. The resistor R33 and capacitor C11 form a RC timer circuit that holds the latch drivers in reset state for 16 seconds after a reset signal from [WD_RST]. The system resets the entire BP/TEMP/NIBP parameter board using the [RESETI\] signal into the PBRST input on the watchdog timer (U18-2).

7.5.4 Memory

The BP/TEMP/NIBP board is programmed with a Flash EEPROM (28F010), U15 via [FLSH_OE\] and [FLSH_WR\] provided by the PAL Decoder, U14. The board uses a 1 megabyte RAM (CXK581000M), U17 via [RAM_OE\] and [RAM_WR\] provided by the PAL Decoder, U14. It consists of seventeen (17) address lines and eight (8) data lines. The memory works in concert with the microprocessor, U16.

7.5.5 Latch Drivers

All the parameters on the board are driven by signals switched through the latch drivers U6 and U7. Each latch has four outputs. U6 [OUT1] and [OUT2] control the select bits [MUXA] and [MUXB] to the multiplexer (U9), used in the Invasive Blood Pressure (IBP) parameter. U6 [OUT3] controls the Noninvasive Blood Pressure (NIBP) pump, and [OUT4] delivers the [ADULT/NEO] select line for the NIBP. U7 [OUT1] is a spare signal line, labeled as [CAL_SW]. U7 [OUT2] controls the Temperature #1 excitation transistor switch, [T1EXC_SW]. Please note that the software directs the excitation voltage to be always switched on. U7 [OUT4] controls the NIBP valve. U19 pin 7 is the high side voltage switch for the pump and valve. U19 is controlled by the [OE5800\] line from the PAL decoder.

7.5.6 Analog-to-Digital Converter

The analog voltage outputs from different parameters run to the 8-channel Analog-to-Digital Converter (ADC), U10. The ADC is controlled by the microprocessor through [DIN] from the TXS (U16-55) on the microprocessor. The ADC uses the [SCLK] and [ACLK] signals for timing in converting the analog data to digital and for communicating with the DBUS interface. The output of the converter is a serial digital data line [DOUT], which is connected to the MPU's RXS line, U16-56. The microprocessor signals the ADC that it is ready to receive data from RTSO\ (U16-45) through the signal [ADCS\], which is connected to CS\, (U10-15).

7.6 Regulators

U12 and U13 are used to regulate -15 V and +15 V down to -12 V and +12 V respectively. The ±12 V supplies are used throughout the BP/TEMP/NIBP Board. The +12 V is further regulated to +5 V_REF by U11.

7.7 NIBP Diagnostics

The following procedures present basic diagnostic tests that should be performed to verify the integrity of the NIBP parameter.

7.7.1 Calibration Check Procedure

Calibration of the monitor should be checked at least once a year, or when there is doubt about the validity of the pressure readings. The test procedure is designed to confirm the accuracy of the monitor as well as to diagnose pneumatic leaks.

> **WARNING: Calibration tubing should always be kept dry and free of particulate matter. Moisture or foreign substances introduced into the pneumatic system can cause damage to the unit.**

The following equipment will be necessary to perform the calibration check procedure:

- A calibrated Mercury (Hg) Manometer
- MDE Calibration Kit
- NIBP Cuff & Hoses

To perform a calibration check, follow these steps:

1. Make sure the NIBP parameter is displayed in one of the waveform display areas. If you need instructions on displaying a parameter in a waveform area, see Chapter 5, "Setup and Operation" of the ESCORT II 300 Operator's Manual.
2. Locate the NIBP calibration kit that was supplied with the ESCORT II.
3. Connect a mercury manometer to the monitor using the calibration kit as shown in Figure 7-3.
4. Wrap the NIBP cuff around a sturdy cylindrical device.
5. Press the NEXT PAGE key twice to display the second SYSTEM SETUP page.
6. Press the TEST softkey.
7. Press the NIBP TEST softkey twice, until CHECK is highlighted.
8. Press the PAGE HOME key. The following is displayed in the NIBP message field:

   CHECK CUF = *XX* **(Note: *XX* indicates any numeric value)**

9. Open manometer to air and verify that the message displayed on the monitor is as follows:

   CUFF = 00

10. Close the valve on the manometer inflation bulb.

11. Using the inflation bulb, manually pump up the pressure to 100 mmHg. The display message should now read:

    CUFF = 100 (± 2%)

12. Using the inflation bulb, manually pump up the pressure to 200 mmHg. The display message should now read:

    CUFF = 200 (± 2%)

13. Repeat the test if pressures indicated are not within the specified tolerances. If the results continue to be out of tolerance, the monitor needs to be recalibrated and should be referred to qualified technical service personnel.

14. To exit the CHECK mode, press PAGE HOME then repeat steps 4 and 5 followed by pressing NIBP TEST until OFF is selected.

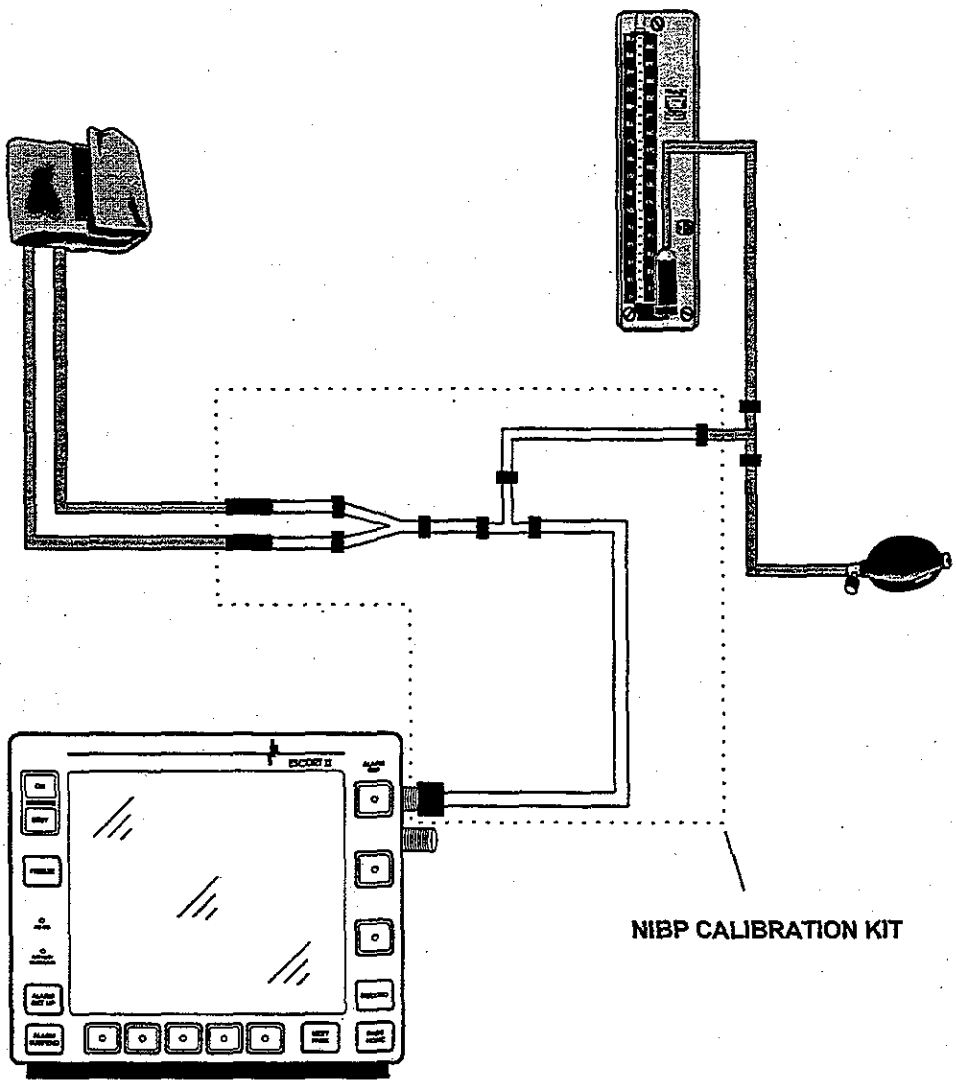


Figure 7-3: NIBP Calibration Check Setup

7.7.2 Leak Test Procedure

If a leak is suspected, use the cuff and hose in question and take the following steps:

1. Wrap the cuff tightly on itself.
2. Press the NEXT PAGE key twice to display the second SYSTEM SETUP page.
3. Press the TEST softkey.
4. Press the NIBP TEST softkey until LEAK is displayed in the highlighted area of the function key.
5. Press the PAGE HOME key.
6. Press the NIBP softkey to display the first NIBP SETUP page.
7. Press the START softkey. The following message is displayed:

   LEAK TEST

8. The ESCORT II will inflate the cuff to 240 mmHg. Be careful not to touch the cuff during inflation. It will then automatically check for a leak. If no leak is detected, a **NO LEAK** message is displayed. If a leak is detected, a **LEAK** message is displayed, and the cuff/hose should be replaced or repaired by technical service personnel before using it to monitor a patient.
9. To exit the LEAK test mode, press PAGE HOME and then repeat steps 2 and 3 followed by pressing NIBP TEST until OFF is selected.

7.7.3 Oscillation Waveform Test Procedure

If the ESCORT II is configured with a recorder, the oscillation waveform and other analysis data can be recorded by taking the following steps:

1. Take an NIBP reading.
2. Press the NEXT PAGE key twice to display the second SYSTEM SETUP page.
3. Press the TEST softkey.
4. Press the NIBP REC START softkey.
5. The oscillation waveform and analysis data will record for the most recent NIBP reading. The record strip will be long and will automatically stop when the analysis is done. The strip should be given to qualified technical service personnel for interpretation.
6. Repeat the above steps for oscillation waveform analyses of any successive NIBP readings.
7. To exit the Oscillation Waveform Test, press the PAGE HOME and then repeat steps 2 and 3 followed by pressing the NIBP TEST key until OFF is selected.

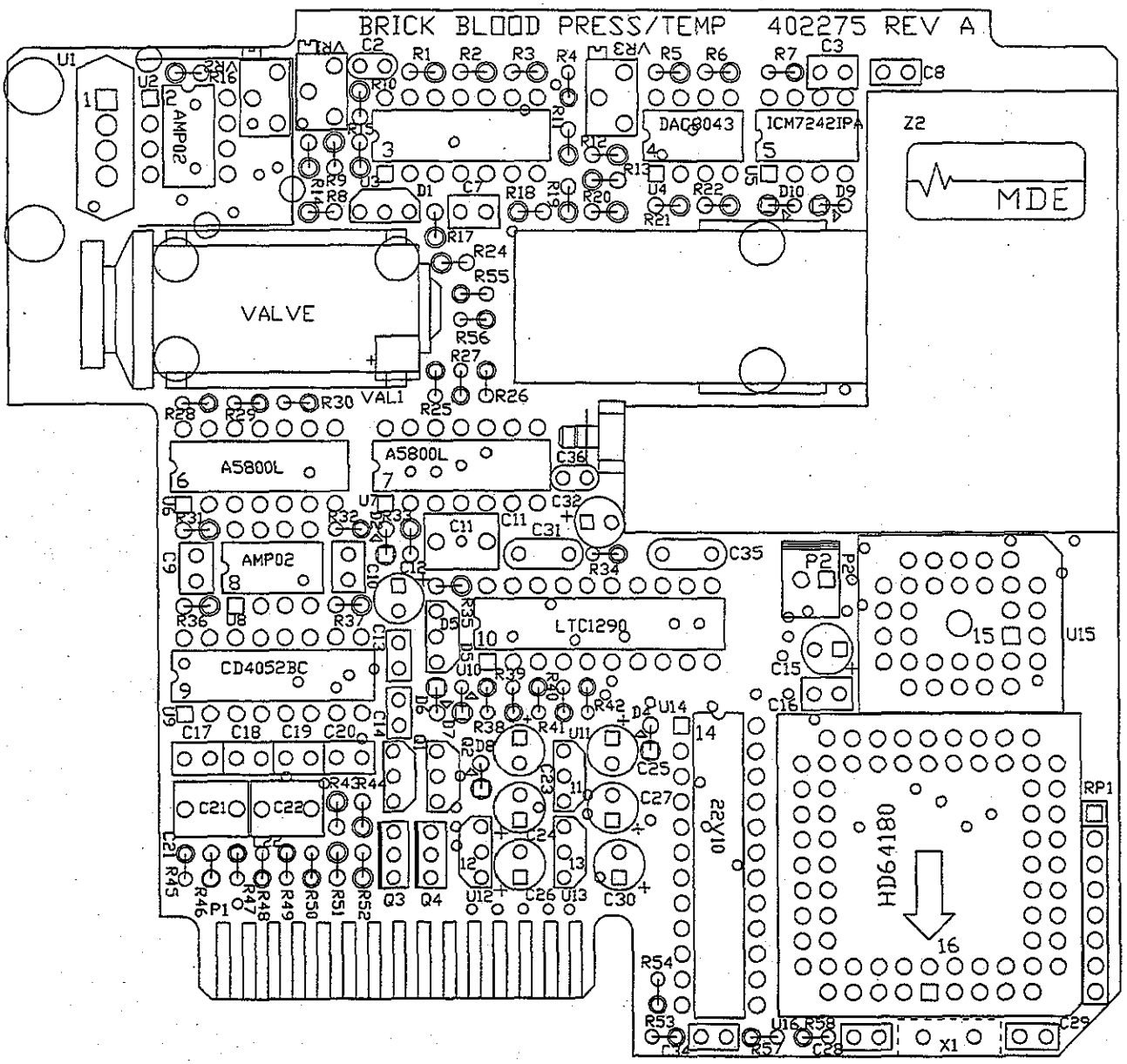


Figure 7-4: BP/TEMP/NIBP Board Layout

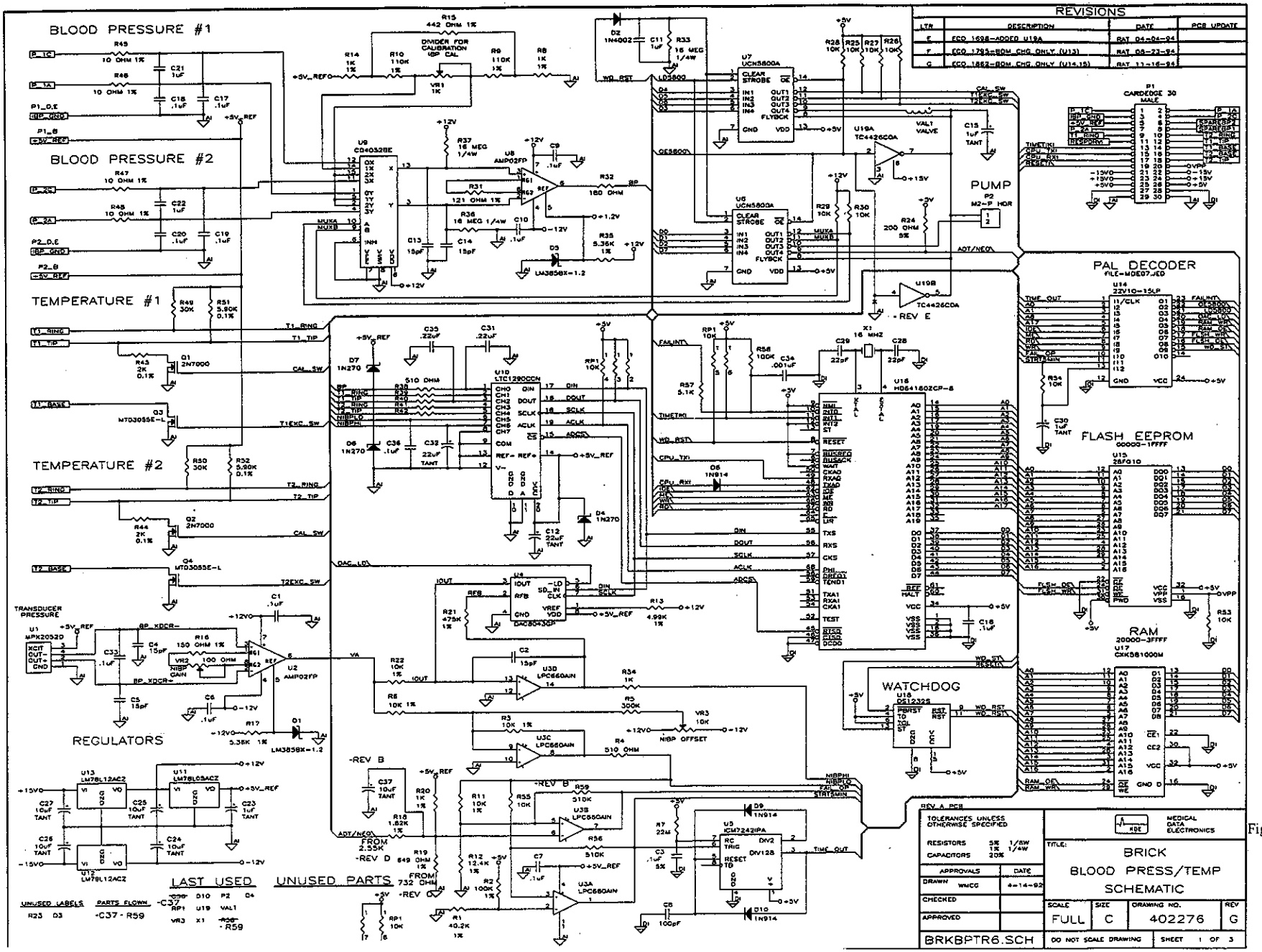


Figure 7-5: BP/TEMP/NIBP Schematic 7-11 / 7-12

Table 7-1: Parts Listing, PCBA P/N 402276-0000, BP/TEMP/NIBP Board (1 of 3)

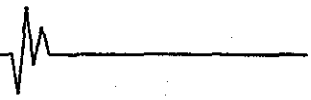
MDE Part Number	Description	Quantity	Reference
352100-0101A	CAP, 100PF,25V,10%,RAD,NPO - .1 LEAD SPACING T & R	1	C8
352100-0150A	CAP, 15PF,50V,10%,RAD,NPO EDPT TAPE & REEL	3	C2, 13, 14
352100-0220A	CAP, 22PF,50V,10%,RAD,NPO EDPT TAPE & REEL	2	C28, 29
352100-0224A	CAP, .22UF,50V,10%,RAD,X7R TAPE & REEL	2	C31, 35
352101-0150A	S*CAP, 15pF,5%,50V,CER NPO 0805	2	C4, 5
352300-0020A	CAP., 1UF,63V,5%,MYLAR	3	C11, 21, 22
352300-0102A	CAP, 1000PF,50V,20%,RAD,MYLAR	1	C34
352300-0104A	CAP, .1UF,50V,20%,RAD,MYLAR	9	C7, 9, 10, 16, 17, 18, 19, 20, 36
352301-0104A	CAP, .1UF,5%,MYLAR BULK ONLY	1	C3
352400-0105A	CAP,1UF,50V,20%,RAD,TANT, MAX:HT .28; O.D. .16 T&R	3	C15, 23, 30
352400-0106A	CAP, 10UF,25V,20%,RAD,TANT	4	C24, 25, 26, 27
352400-0226A	CAP, 22UF,25V,20%,TANT T & R	2	C12, 32
352403-0106A	CAP, 10uF,5%,12V(OR HIGHER),RAD,TANT	1	C37
352600-0043A	S*CAP, 0.1uF,10%,50V,CER X7R 1206	3	C1, 6, 33
354000-0138A	CONN, 2-P,M,STRT LOCK,.1 CTR,HDR	1	P2
356000-0026A	XTAL, 16MHZ, LOW PROFILE, .142IN X .425IN	1	X1
364000-0055A	IC, CD4052,DIP	1	U9
364000-0109A	IC, 78LO5 +5V REG. TO-92 PKG.	1	U11
364000-0199A	S*IC, Z80180 8/10MHZ PLCC	1	U16
364000-0207A	IC, LM78L12ACZ,+ 12V REG TO92	1	U13
364000-0208A	IC, LM79L12ACZ NEGATIVE 12V VOLTAGE REG LOW PWR	1	U12
364000-0210A	IC, LTC1290CCN	1	U10
364000-0211A	IC, AD620BN OP AMP	2	U2, 8
364000-0248A	IC, UCN5800A,BIMOS LATCHED DRIVER	2	U6, 7
364000-0249A	IC, LPC660AIN, CMOS QUAD OP AMP 8PIN DIP PKG	1	U3
364000-0250A	IC, 22V10-10,PAL,24-PIN DIP	1	U14 - NEEDS PROGRAM
364000-0251A	IC, ICM7242IPA,TIMER COUNTER 8-PIN DIP PKG	1	U5
364000-0252A	IC, DAC8043GP,DIG TO ANAL CONV,8PIN DIP(P OR Z PK)	1	U4

Table 7-1: Parts Listing, PCBA P/N 402276-0000, BP/TEMP/NIBP Board (2 of 3)

MDE Part Number	Description	Quantity	Reference
364000-0253A	IC, TC4426COA,1.5A DUAL HIGH DRIVER 8PI SOIC PKG	1	U19
364000-0266A	S*IC, CXK581000M,8BIT,HS STATIC RAM,32-PIN,SOP	1	U17
364000-0277A	S*IC, WATCHDOG,16-PIN SOIC SMD	1	U18
364000-0278A	S*IC, 1 MEG,UNSECT FLASH PROM PLCC 32,SMD	1	U15 - NEEDS PROGRAM
365000-0008A	SKT, 8-POS,DIP,TIN PLATE,L.P.	4	SU2, 4, 5, 8
365000-0014A	SKT, 14-POS,DIP,TIN PLATE,L.P.	1	SU3
365000-0016A	SKT, 16-POS,DIP,TIN PLATE,L.P.	1	SU9
365000-0020A	SKT, 20-POS,DIP, TIN PLATE,L.P.	1	SU10
365000-0068A	S*SKT, 68-PIN PLCC	1	SU16
365000-0132A	S*SKT, 32-PIN, PLCC	1	SU15
365000-0224A	SOCKET, 24 PIN DIP	1	SU14
370100-0166A	RES, 16M,1/4W,5%,CF TAPE & REEL	3	R33, 36, 37
370100-0201A	RES, 200,1/4W,5%,CF TAPE & REEL	1	R24
370100-0226A	RES, 22M,1/4W,5%,CF TAPE & REEL	1	R7
370100-0304A	RES, 300K,1/4W,5%,CF TAPE & REEL	1	R5
370101-0102A	RES, 1K,1/8W,5%,CF TAPE & REEL	1	R34
370101-0103A	RES, 10K,1/8W,5%,CF TAPE & REEL	2	R54, 55
370101-0103A	RES, 10K,1/8W,5%,CF TAPE & REEL	7	R25, 26, 27, 28, 29, 30, 53
370101-0104A	RES, 100K,1/8W,5%,CF TAPE & REEL	1	R58
370101-0181A	RES, 180,1/8W,5%,CF TAPE & REEL	1	R32
370101-0303A	RES, 30K,1/8W,5%,CF TAPE & REEL	2	R49, 50
370101-0511A	RES, 510,1/8W,5%,CF TAPE & REEL	6	R4, 38, 39, 40, 41, 42
370101-0512A	RES, 5.1K,1/8W,5%,CF TAPE & REEL	1	R57
370101-0514A	RES, 510K,1/8W,5%,CF TAPE & REEL	1	R56
370101-0514A	RES, 510K,1/8W,5%,CF TAPE & REEL	1	R59
370200-1001A	RES, 1K,1/4W,1%,MF TAPE & REEL	3	R8, 14, 20
370200-1002A	RES, 10K,1/4W,1%,MF TAPE & REEL	4	R3, 6, 11, 22
370200-1003A	RES, 100K,1/4W,1%,MF TAPE & REEL	1	R2
370200-1103A	RES, 110K,1/4W,1%,MF TAPE & REEL	2	R9, 10
370200-1210A	RES, 121,1/4W,1%,MF TAPE & REEL	1	R31

Table 7-1: Parts Listing, PCBA P/N 402276-0000, BP/TEMP/NIBP Board (3 of 3)

MDE Part Number	Description	Quantity	Reference
370200-1242A	RES, 12.4K,1/4W,1%,MF TAPE & REEL	1	R12
370200-1500A	RES, 150,1/4W,1%,MF TAPE & REEL	1	R16
370200-1821A	RES, 1.82K,1/4W,1%,MF TAPE & REEL	1	R18
370200-4022A	RES, 40.2K,1/4W,1%,MF TAPE & REEL	1	R1
370200-4412A	RES, 442,1/4W,1%,MF TAPE & REEL	1	R15
370200-4753A	RES, 475K,1/4W,1%,MF TAPE & REEL	1	R21
370200-5361A	RES, 5.36K,1/4W,1%,MF TAPE & REEL	2	R17, 35
370200-6490A	RES, 649,1/4W,1%,MF TAPE & REEL	1	R19
370202-1000A	RES, 10,1/8W,1%,MF TAPE & REEL	4	R45, 46, 47, 48
370202-4991A	RES, 4.99K,1/8W,1%,MF TAPE & REEL	1	R13
370204-5901A	RES, 5.90K,1/4W,0.1%,MF TAPE & REEL	2	R51, 52
370205-2001A	RES, 2K,1/20W,0.1%,MF (+/-50ppm/DEG C)	2	R43, 44
370300-0017A	RES, SIP,10K,5%,8-LEAD,7-COMP,COMMON	1	RP1
374300-0101A	POT, 100,10-TURN,VAR,SIDE-ADJ	1	VR2
374401-0103A	POT, 10K,TRIMM,MULTI-TURN,CERMET FILM (860X)	1	VR3
374402-0102A	POT, 1K,10-TURN,SIDE ADJ	1	VR1
376000-0019A	XSTR, 2N7000,FET	2	Q1,2
376000-0021A	XSTR, MTD3055E-1 N CHANNEL FET,8 AMP,60V	2	Q3, 4
378000-0001A	DIO, 1N270 T&R	3	D4, 6, 7
378000-0002A	DIO, 1N4002GP,RCTFR, (MOT ONLY) T&R	1	D2
378000-0005A	DIO, 1N914,SIGNAL T&R	3	D8, 9, 10
378000-0068A	DIO, LM385Z-1.2,LOW PWR VOLT REF	2	D1, 5
402275-0000	PCB, BRICK NIBP/BP/TEMP REV A (E1600)	1	-



8

CO2 & CO2 Processor Boards

8.1 Overview

The ESCORT II CO_2 system is comprised of three major components, as listed below.

- Optical Bench (CO_2 Sensor)
- CO_2 Main Board
- CO_2 Processor Board

The Optical Bench, or CO_2 sensor, is the interface between the patient and the ESCORT II bedside monitor, and is placed in the patient airway. The CO_2 Board processes the $ETCO_2$ information received from the Optical Bench while also providing sensor heat-up and control. The CO_2 Processor Board is the digital interface between the CO_2 board and the ESCORT II's main CPU board.

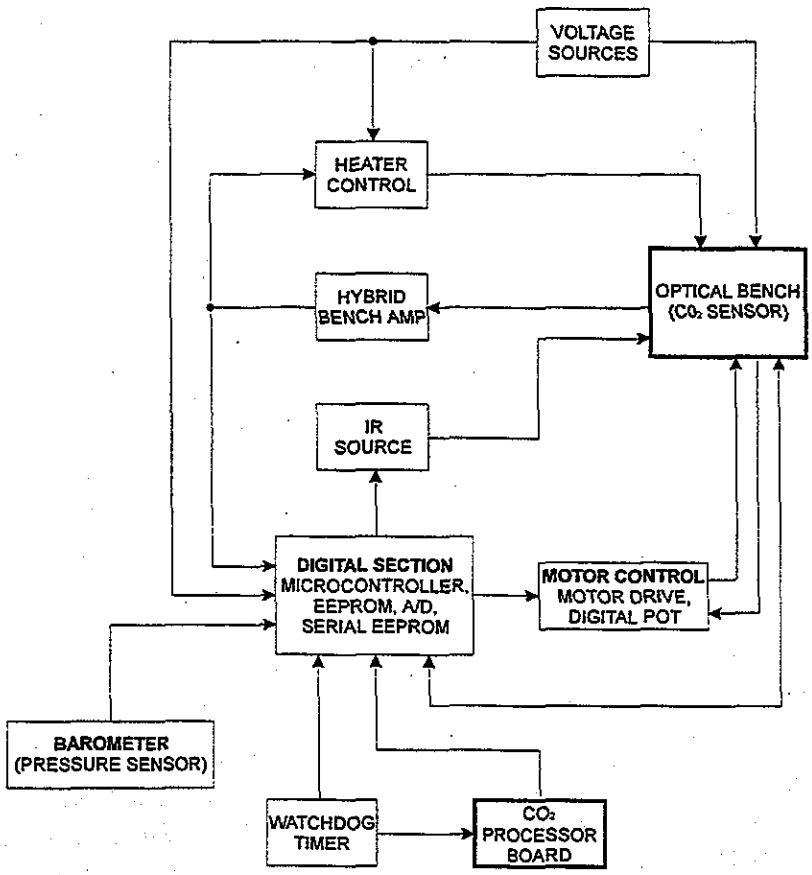


Figure 8-1: CO_2 Block Diagram

8.2 Optical Bench (CO_2 Sensor)

The CO_2 sensor consists of a light source, a photo detector, an infrared filter, and chopper wheel which contains a sample gas cell. The same type of CO_2 sensor is used in both mainstream and sidestream applications. The sensor is factory calibrated to characterize its response to CO_2. At 42° C, the sensor is exposed to known CO_2 concentrations and the resulting measurements are sent to the CO_2 processor, along with the ambient barometric pressure. The sensor's CO_2 measurements are then compared to the known concentrations, yielding sensor specific calibration coefficients. These coefficients become part of the calibration equation that is used to determine CO_2 levels during patient monitoring. All calculations are performed by internal software.

WARNING: Great care must be exercised in handling the CO_2 sensor. There are no serviceable parts inside the sensor. If the sensor malfunctions, contact MDE Technical Support.

WARNING: DO NOT immerse, gas sterilize, or autoclave the sensor; doing so will cause damage to the sensor which is NOT COVERED by the product warranty.

8.3 CO_2 Board

The CO_2 Board consists of eight sections, each section is listed below and discussed in the following text.

- Bench Amplifier Hybrid
- Heater Control
- Motor Drive Hybrid
- Barometer Sensor
- IR LED / IR Source
- Digital Section
- Watchdog Timer
- Regulators/Converters

8.3.1 Bench Amplifier Hybrid

The Bench Amplifier Hybrid (J2) is an OEM module which functions as an interface between the Optical Bench (CO_2 Sensor) and the CO_2 Board. The Bench Amplifier's functions include amplification of the sensor detector output, and accurate biasing of the detector so that its output is zero referenced and within the range of the analog-to-digital converter (U4). The Bench Amplifier Hybrid module is soldered directly to the CO_2 Board. It is not a serviceable assembly, and is replaced as a module if defective.

The actual CO_2 data originates on the Optical Bench (CO_2 sensor). It is a rounded trilevel signal, and is called [DETECT]. See Figure 8-2 for details. The three levels of the [DETECT] signal are REFERENCE, DARK, and KIDNEY. The voltage level of the REFERENCE signal is approximately 0.8 VDC; DARK is about 0 V, and KIDNEY is approximately 1.5 VDC, depending on actual CO_2 level. The [DETECT] signal is routed to the Hybrid Bench Amp where it is amplified and filtered before being routed back into the CO_2 Board as [VSIG] at (J2-10). [VSIG] is sent to the microcontroller (U10-1) and is used to produce the [DARK] signal (U10-7). [DARK] is sent back into the Bench Amp Hybrid at (J2-11) and is used to control [-BIASDRV].

[-BIASDRV] is an output from the Bench Amp (J2-14) which is controlled by the [DETECT] and [DARK] signals. Its voltage level varies according to the [DETECT] and [DARK] signals to compensate for the changes in measurements. However, the ratio of the measurements does not change. This feature is crucial in obtaining stable and reliable measurements despite normal variability in system components. The [-BIASDRV] is photo-coupled to U13 and filtered by C18 and C19 to produce the [-BIAS] signal. The [-BIAS] signal varies from -36 V to 0 VDC, with a typical level being in the -10 V range.

The temperature of the sensor is fed back into the Bench Amplifier Hybrid as the signal [THERM] at J2-2. It is a low level signal of approximately 0.7 VDC. On the Bench Amplifier Hybrid, [THERM] is amplified and exits as [TEMP], which has a level between 0 V and approximately 2.5 VDC, with the level being approximately 2.4 VDC at 42° C.

The Bench Amplifier Hybrid receives its supply voltages of +5 VA and -5 VA from the main CO_2 Board.

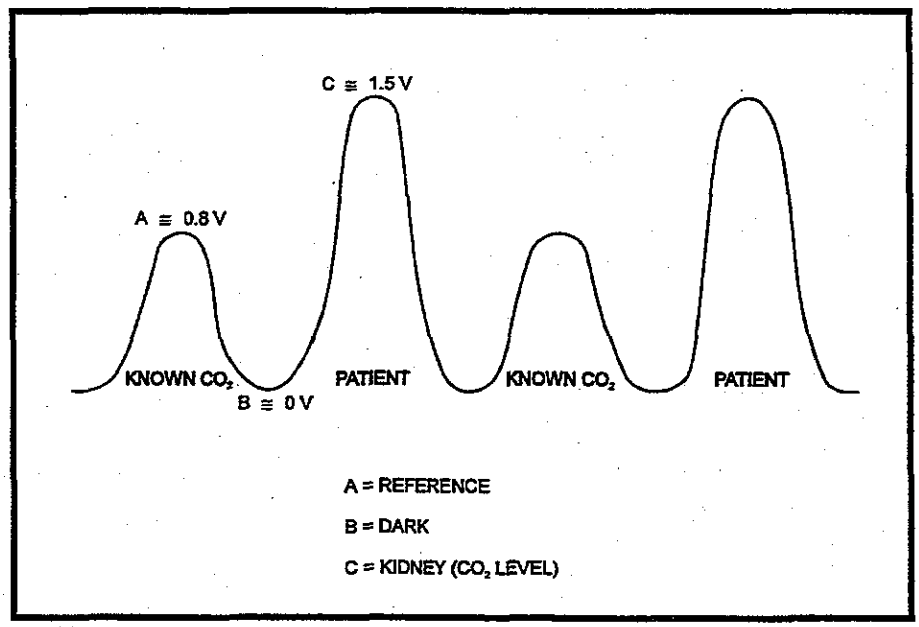


Figure 8-2: CO_2 Output Signal

8.3.2 Heater Control

The Heater Control is provided by the signals [HEATPWM] and [HFLT]. The pulse width modulator [HEATPWM] signal is originated from the microcontroller U10-4 under program control. The [HEATPWM] signal is used to drive the heater in the sensor. It goes into the inverter (U17B) and, if the heater temperature is between 0° C and 48° C, it passes through U17B, and is then inverted by U17D. The current driver (U18) outputs current to drive the heater. It is then EMI-filtered by L1 and C24, and is routed to the sensor heater as the signal [HEATER].

U6A and U6B are window detectors for the sensor's heater temperature. If the [TEMP] signal at the inverting input of U6A rises above 2.85 VDC (which is the reference voltage set at U6-3 that corresponds to 48° C at the sensor), the output at U6-1 goes low. U6B is used to detect a temperature approaching 0° C, which is an indication that there is no sensor connected. If the [TEMP] signal goes below 0.8 VDC (the reference voltage set at U6-6), the output at U6-7 goes low. U6-1 and U6-3 are then inverted by U17A, and become the signal [HFLT]. If [HFLT] goes high, it blocks the [HEATPWM] signal from passing through U17B. Furthermore, [HFLT] is then routed to the microcontroller (U10) to stop the [HEATPWM] output at U10-4.

8.3.3 Motor Drive Hybrid

The Motor Drive Hybrid (J1) is an OEM module which functions as an interface between the optical bench motor and the CO_2 Board. The microcontroller (U10) on the CO_2 Board routes control signals to the optical bench motor through the Motor Drive Hybrid. It takes in [DRIVE], [SENSE], [KICK], [MTRGATE], [MTRCLK], [VH], [VREF], and [VW] signals. The signal [KICK] comes from the microcontroller (U10-8). When the microcontroller prepares to start the motor, it generates a short pulse called [KICK], which enters the hybrid motor driver at J1-2, and outputs to the motor driver at J1-1, [DRIVE]. The purpose of [KICK] is to align the motor in the sensor so that it spins in the right direction, and it occurs only once during the start-up phase of the CO_2 process.

The amplitude of the motor drive signal is controlled by the digital potentiometer, U2. [VH] is the high side of the digital potentiometer and is a result of the processing of [VREF] on the motor drive hybrid. The wiper setting, [VW], is programmed into the serial EEPROM (U5) during factory configuration. The actual driving of the motor is done via the output of the motor drive hybrid at J1-5, where it goes through the current drivers Q2 and Q3. The output of Q2 and Q3 become the signal [DRIVE], and is the actual driver for the motor in the sensor.

Once the [KICK] signal occurs, it is detected by the microcontroller (U10), which then generates a pulse train [MTRCLK]. [MTRCLK] is the reference for the motor speed control on the motor drive hybrid. The signal [DRIVE], in addition to driving the motor, is fed back to the hybrid motor driver, and is compared to the signal [SENSE]. [SENSE] is a low level ramp which is generated by a sense coil on the sensor motor assembly.

When the motor is spinning, the signal [MTRGATE], originating from the microcontroller (U10-9), is at 0 VDC. If the microcontroller detects an error, [MTRGATE] goes to +5 VDC, blocking the motor drive signal on the hybrid motor driver, and shutting down the motor.

8.3.4 Barometer Sensor

The Barometer Sensor circuit generates a voltage proportional to the atmospheric pressure by applying a constant current source to the pressure transducer (U1). U7A generates an output voltage proportional to the atmospheric pressure. The current inputs at U1-4, while U7-2 provides a return path. Internally, U1 is a resistive bridge. The internal connections of U1-4 to U1-3, and U1-1 to U1-2 produce fixed resistances. The internal connections of U1-4 to U1-1, and U1-1 to U1-2 produce variable resistances. U1-3 develops a reference voltage of 7.3 VDC. U1-1 is a voltage proportional to the atmospheric pressure. This is buffered by U7B, and is summed at U7D. U7-14 delivers a voltage proportional to the pressure level which is applied to the microcontroller (U10-64) for calculations of the barometric pressure.

8.3.5 IR LED / IR Source

An infrared LED resides in the sensor head. It is the source used for generating the [DETECT] signal. Once the sensor motor reaches optimal speed, U10 activates the [SOURCEON] line at U10-10. U10 does not have the capability to drive the IR LED, therefore [SOURCEON] is used as a control signal for U8, which is a constant current source. When [SOURCEON] goes high (active), it turns on U10, which outputs the signal [SOURCE] which drives the IR LED. The [SOURCE] signal is approximately 1.25 VDC, and supplies the IR LED with about 83 mA.

8.3.6 Digital Section

The Digital Section consists of a microcontroller (U10), which operates at about 11.059 MHz. It also consists of a 1-megabyte flash PROM (U16), an octal address latch with tri-state outputs (U11), a 1024-bit serial EEPROM (U5), an analog-to-digital converter (U4), and some discrete logic gates.

The microcontroller, U10, has five addressable ports. Each of which consists of eight lines. Port 0 consists of eight data lines, [AD0 through AD7]. It is the multiplexed low order address bus and data bus. During the address cycle, the address latch (U11) receives the address, and is latched on its Q outputs by the [ALE] signal from U10-48.

Port 1 consists of four capture timing input signals for timer T2. Only CT0 is used on the main CO_2 board as [MTRCLK], the other three capture timing inputs are left open. The T2 event input produces the output [I2CCLK] on U10-20; the T2 timer reset signal outputs [I2CDAT] on U10-21; the serial port clock line outputs [EECLK] on U10-22; and the serial port data line outputs [EEDAT] on U10-23.

Port 2 outputs eight high order address bytes used during external memory accesses. The address and data lines communicate with the flash PROM (U16), which contains the CO_2 control program.

Only three lines are used in Port 3 for our application, namely, receive data line on U10-24, transmit data line on U10-25, and timer 1 external input line on U10-29, which is the signal [HFLT].

Port 4 is used by timer 2. The first five lines of Port 4 are used by timer T2 to compare and set/ reset outputs on a match with timer T2. In our case, these five lines are [DARK] on U10-7, [KICK] on U10-8, [MTRGATE] on U10-9, [SOURCEON] on U10-10, and [NVCS] on U10-11. The other three lines in Port 4 are used to compare and toggle outputs on a match with timer T2. These three lines are [POTCS] on U10-12, [ADCS] on U10-13, and [EECS] on U10-14.

Port 5 consists of eight analog-to-digital converter inputs. Only six lines are used: [VSIG] on U10-1, [TEMP] on U10-68, [SOURCE] on U10-67, [+BIAS] on U10-66, [HEATER] on U10-65, and [PRESSURE SENSOR] on U10-64. Port 5 receives controls signals for its closed loop operations. [HEATER] is the feedback for [HEATPWM]. [SOURCE] is the feedback for [SOURCEON], and [+BIAS] is the feedback for [BIASPWM]. U10-29 is an input which monitors the [HFLT] line. When [HFLT] is high, it shuts down the [HEATPWM] signal. U10-68 monitors the sensor temperature via the [TEMP] signal.

The Address Latch Enable line, [ALE], is on U10-48. It latches on the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. The Program Store Enable line, [PSEN\], is on U10-47. When it is low, it reads strobe to external program memory. The PROM, U16, and the octal latch, U11, work in concert with these two lines to provide the microcontroller, U10, with proper instructions.

U10 also performs the task of controlling the A/D converter, serial EEPROM (U5), and the digital potentiometer (U2). The A/D converts the [VSIG] information, which is the CO_2 data, into 10-bit serial information, which is then supplied to the microcontroller at U10-21 as [I2CDAT]. [VSIG] also supplies the microcontroller at U10-1, and is used as a signal reference.

The serial EEPROM (U5) contains the sensor probe compensation information and is programmed by the factory. During CO_2 start-up, this information is placed on the serial bus [I2CDAT], and is selected by the signal [NVCS].

8.3.7 Watchdog Timer

The watchdog timer (U19) is used to reset the microcontroller (U10) if it becomes stuck or inactive. It is strobed continually by the signal [TXD], which originates on the CO_2 Processor Board. If the watchdog is not strobed once every 1.2 seconds, [RESET] and [RESET\] become active, resetting the microcontroller.

The watchdog timer also functions as a power monitor. If the supply voltage (+5 VDC) falls below 4.5 VDC, [RESET] and [RESET\] become active, causing the microcontroller to halt operation until the supply voltage returns to normal.

8.3.8 Regulators/Converters

There are four voltages generated on the CO_2 Board, which are derived from the +5 VA voltage and the -15 VISO voltage. U14, U12, and U9 are DC to DC voltage converters.

The voltage level, [-15VISO], is converted to -30 V by the CMOS voltage converter, U14. The -30 V is again converted to -45 V by the CMOS voltage converter, U12. The -45 V is used to bias the opto-isolator, U13, which produces the [-BIAS] signal. D5 blocks any positive voltages from entering and damaging U12. D4 is a 36-volt zener diode, which brings the -45 V line down to -36 VDC, to be used in the -BIAS circuit on the sensor head.

U9 is a voltage inverter, which utilizes the +5 VA at its input, and outputs -5 VA, which is also used on the sensor head.

U3 is a reference voltage generator. It supplies a voltage of about 4.75 VDC to its output at U3-6, [VREF], based on the voltage divider, R2 and R3, at U3-5.

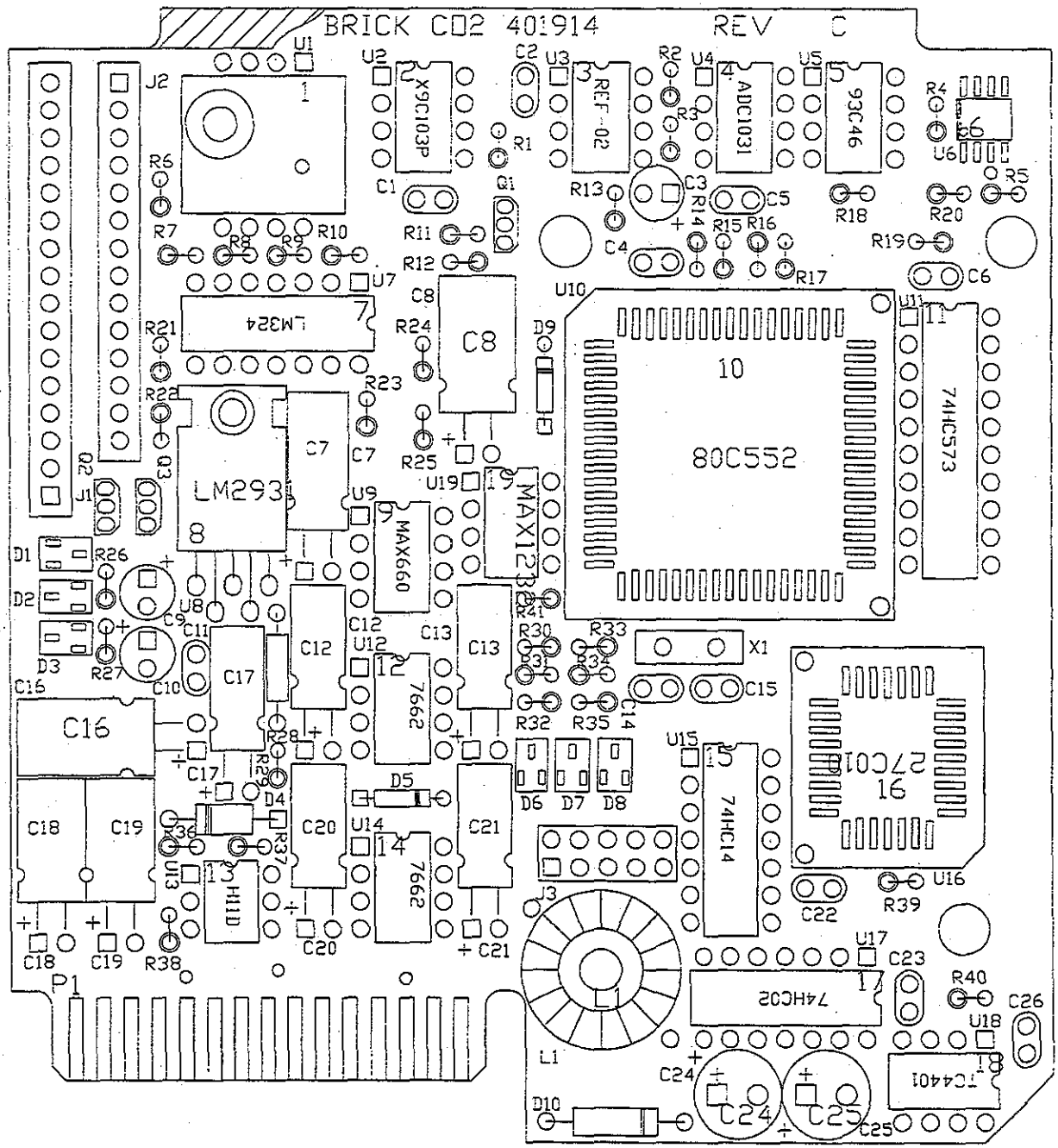


Figure 8-3: CO_2 Board Layout

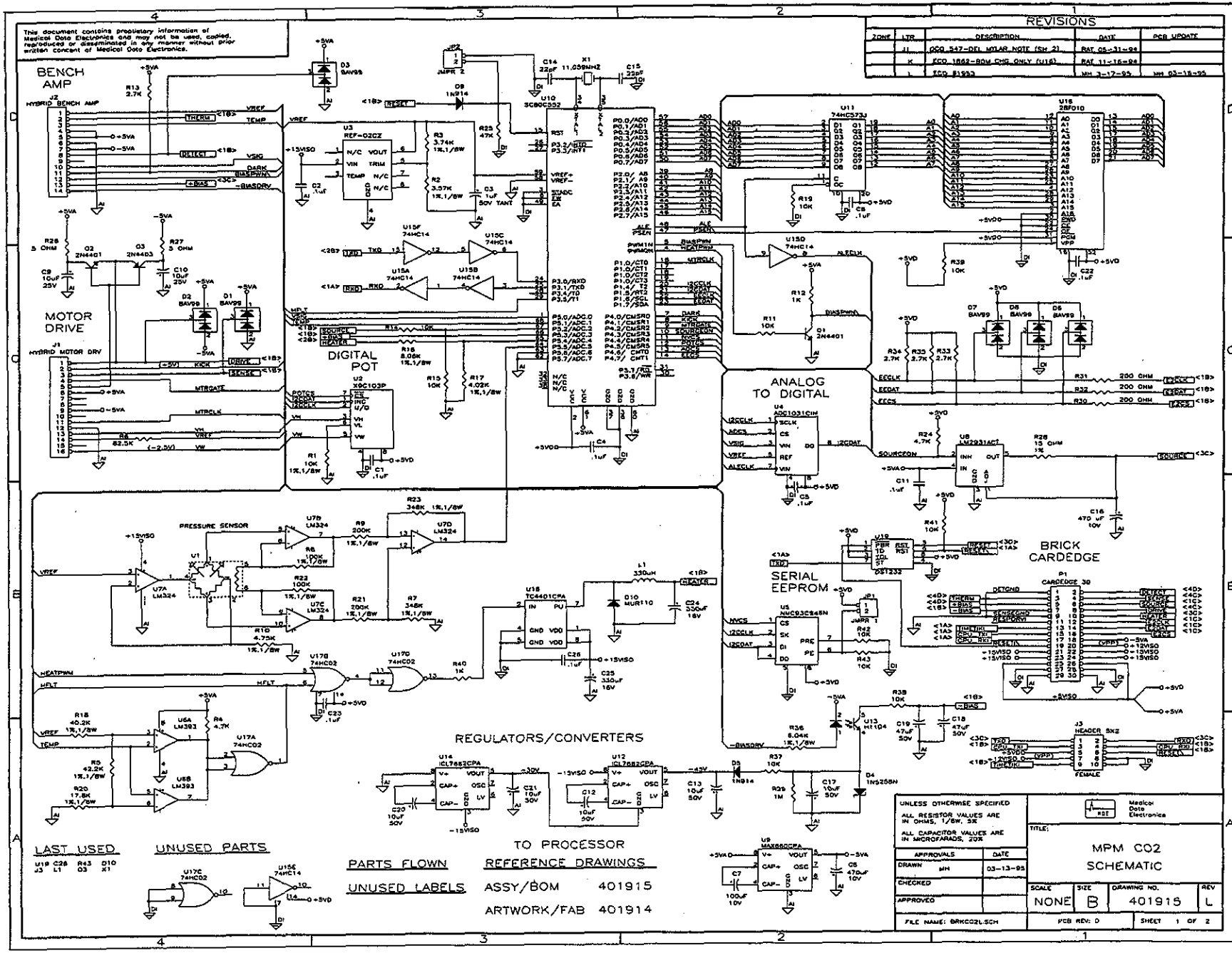


Figure 8-4: CO_2 Schematic 8-9 / 8-10

8.4 CO_2 Processor Board

The CO_2 Processor board acts as an interface between the main CO_2 board and the ESCORT II's main CPU board (see Chapter 4). This board is attached directly to the CO_2 main board and is connected by J1 (CO_2 Processor Board) to J3 (main CO_2 Board).

A 64180 MPU (U4) is employed in conjunction with a 128K EPROM (U3) and a 32K Static RAM (U5). The signal [CLKOUT] is the 8 MHz output of the MPU and may be measured at U4-68. That signal is then routed into U1A-3 and is divided by two producing a 4 MHz square wave at U1A-6. This 4 MHz signal is now referred to as [UP] and serves as an input to U2-5, which is an Up/Down Counter. The [UP] signal gets divided by thirteen to produce an output of approximately 307.69 kHz at U2-12, referred to as [LOAD]. The [LOAD] signal is then used for the clock input to U1B-11. U1B divides [LOAD] by two for the output signal [CKA1] which is approximately 153.8 kHz and is utilized as a signal baud rate generator.

Communication to the main CO_2 board is accomplished by the signals [TXD] and [RXD], (U4-51 & U4-53 respectively) at a baud rate of 9600. Communication to the ESCORT II main CPU board is done with the signals [CPU_TXI] and [CPU_RXI] (U4-48 & U4-49 respectively).

The signal [TIMETIKI] maintains synchronization in the Multiparameter Module (MPM) and is shared by all parameter boards within the MPM. [TIMETIKI] is the isolated version of [TIMETIC] whose frequency is equal to four times (4X) the AC line frequency. A typical 60 Hz system produces a [TIMETIC] frequency of 240 Hz while a 50 Hz system produces a [TIMETIC] frequency of 200 Hz.

8.5 CO_2 Processor with Cardiac Output Board

If the ESCORT II is equipped with both the CO_2 and Cardiac Output options, then the entire CO_2 Processor capability is embedded in the Cardiac Output Board with minor modifications. See Chapter 9 for details on Cardiac Output.

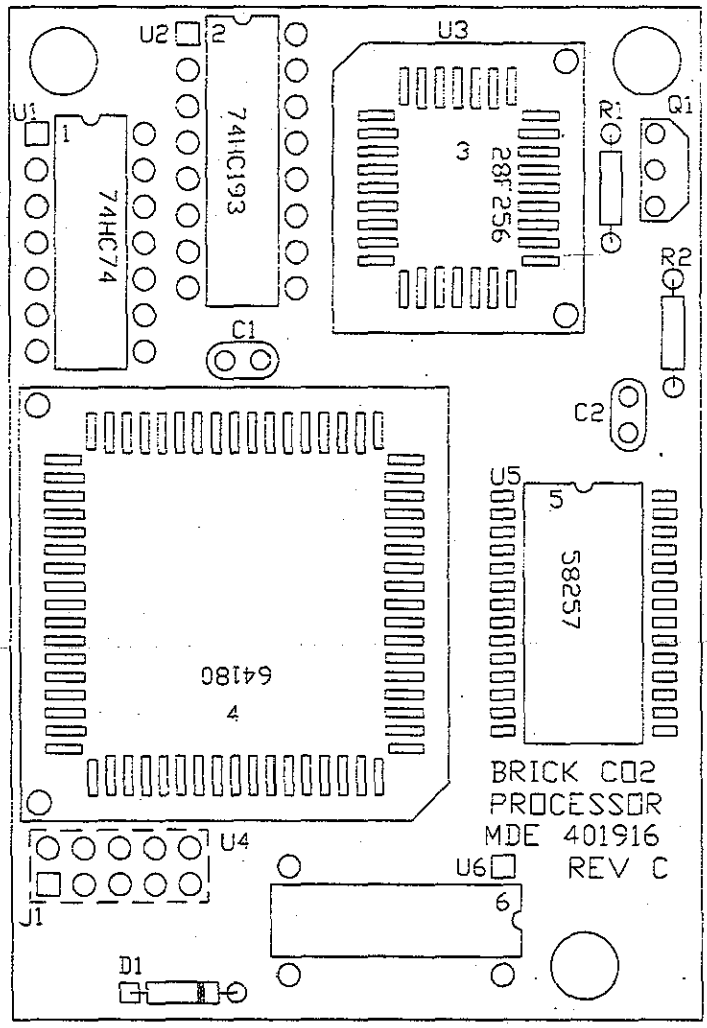


Figure 8-5: CO_2 Processor Board Layout

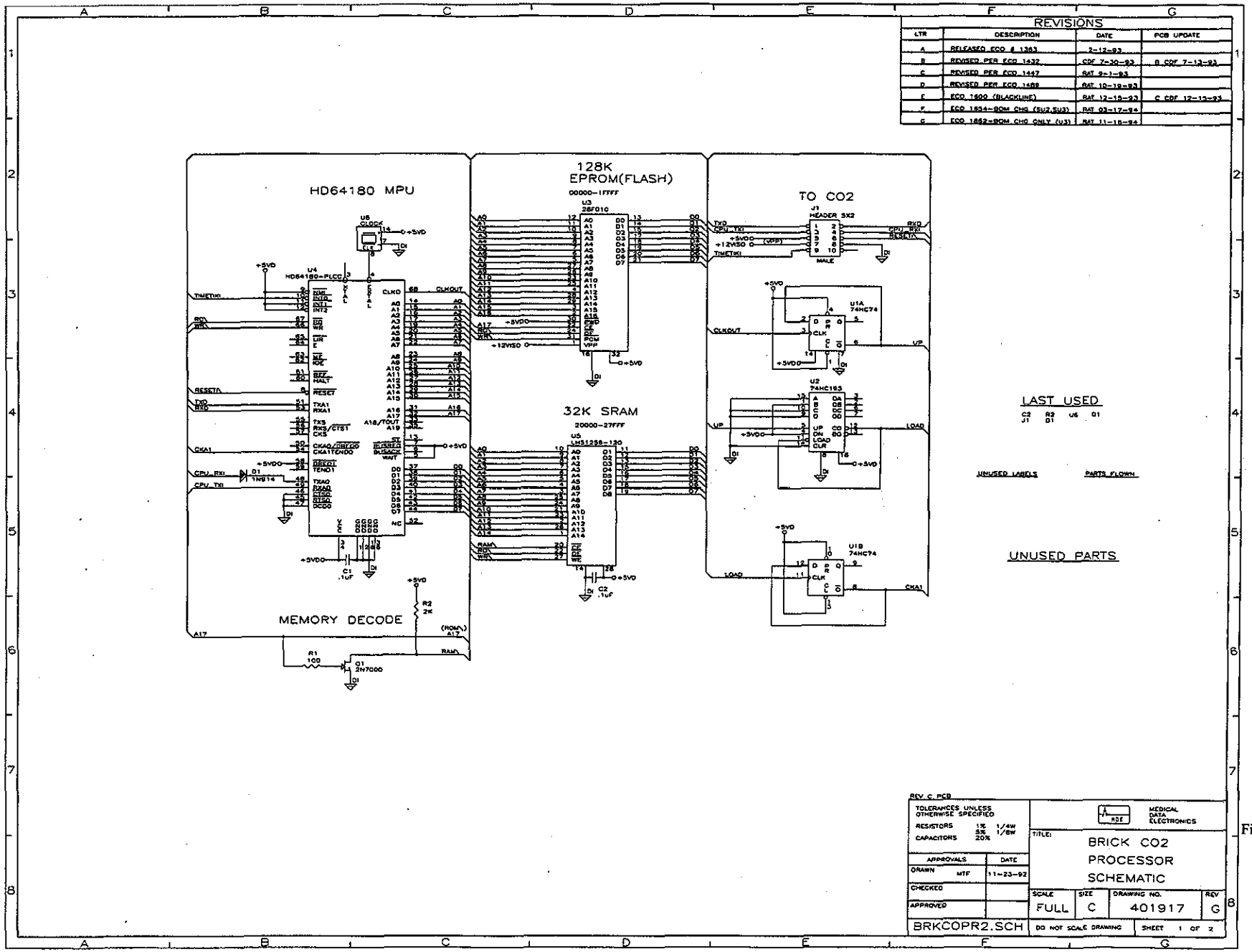


Figure 8-6: CO_2 Processor Schematic
8-13 / 8-14

Table 8-1: Parts Listing, PCBA P/N 401915-0000, CO_2 Board (1 of 3)

MDE Part Number	Description	Quantity	Reference
352100-0104A	CAP, .1UF,50V,10%,RAD,X7R TAPE & REEL	9	C1, 2, 4, 5, 6, 11, 22, 23, 26
352100-0220A	CAP, 22PF,50V,10%,RAD,NPO EDPT TAPE & REEL	2	C14, 15
352200-0476A	CAP, 47UF,25V,RAD,ELECT 2.5mm LEAD SPACE	2	C18, 19
352201-0106A	CAP, 10uF,20%,50V,LOW ESR,RAD,5x11mm,ELECT	1	C17
352201-0106A	CAP, 10uF,20%,50V,LOW ESR,RAD,5x11mm,ELECT	4	C12, 13, 20, 21
352201-0107A	CAP,100UF,10V,RAD,ELECT,.197X.433 CS 2mm LD BULK	1	C7
352201-0337A	CAP, 330UF,16V,ELEC,RAD 3.5mm LEAD SPACE	2	C24, 25
352202-0477A	CAP, 470UF,10V,20%,6.3mmx11mm,RAD,ELECT	2	C8, 16
352400-0105A	CAP,1UF,50V,20%,RAD,TANT, MAX:HT .28; O.D. .16 T&R	1	C3
352400-0106A	CAP, 10UF,25V,20%,RAD,TANT	2	C9, 10
354000-0304A	CONN, 72-PIN,F,.1 CTR,D-ROW SOLDER SNAP-AWAY	5	J3
356000-0027A	XTAL, 11.059 MHZ,LOW PROFILE,HC495 PKG	1	X1
358100-0145A	SCR, 6-32x1/2~LG,NYL,FLT SLT HD 82DEG	1	-
360500-0130A	NUT, HEX,NYLON,6-32	1	-
360500-0141A	STDOFF, 4-40 x 3/16DIA x 5/16LG AL SWAGE GOLD IR	3	-
364000-0057A	IC, LM324, LINEAR	1	U7
364000-0163A	IC, 74HC02	1	U17
364000-0169A	IC, 74HC14	1	U15
364000-0213A	IC, WATCHDOG,8-PIN DIP	1	U19
364000-0254A	IC, 80C552,MICROCONTROLLER,8-BIT,PLCC,16 MHZ	1	U10
364000-0255A	IC, H11D4,OPTO-ISOLATOR,HI VOLTAGE	1	U13
364000-0256A	IC, 74HC573J,OCTAL LATCH,TRI-STATE OUTPUT,DIP	1	U11
364000-0257A	IC, LM2931ACT REGULATOR	1	U8
364000-0258A	IC, ADC1031BIN,A TO D CONVERTOR,10 BIT SERIAL I/O	1	U4
364000-0259A	IC, REF-02CZ,VOLTAGE REF/TEMP XDUCER	1	U3
364000-0260A	IC, ICL7662CPA,CMOS VOLTAGE CONVERTER	2	U12, 14
364000-0261A	IC, TC4401CPA,6 AMP,MOSFET DRIVER,OPEN DRAIN	1	U18
364000-0262A	IC, 93CS46N,EEPROM,1024 BIT SERIAL 8 PIN DIP	1	U5
364000-0264A	IC, MAX660CPA,CMOS VOLTAGE CONVERTER	1	U9

Table 8-1: Parts Listing, PCBA P/N 401915-0000, CO_2 Board (2 of 3)

MDE Part Number	Description	Quantity	Reference
364000-0265A	IC, X9C103P,DIGITAL POT	1	U2
364000-0278A	S*IC, 1 MEG,UNSECT FLASH PROM PLCC 32,SMD	1	U16 - NEEDS PROGRAM
364000-0291A	S*IC, LM393N M08A DUAL VOLT COMPARATOR SMD	1	U6
365000-0168A	S*SKT, 68-PIN,LOW PROF,PLCC W/ LOCATING POSTS,SMD	1	SU10
365000-0232A	S*SKT, 32-PIN,LOW PROF,PLCC W/ LOCATING POSTS,SMD	1	SU16
370101-0102A	RES, 1K,1/8W,5%,CF TAPE & REEL	2	R12, 40
370101-0103A	RES, 10K,1/8W,5%,CF TAPE & REEL	10	R11, 14, 15, 19, 37, 38, 39, 41, 42, 43
370101-0105A	RES, 1M,1/8W,5%,CF TAPE & REEL	1	R29
370101-0201A	RES, 200,1/8W,5%,CF TAPE & REEL	3	R30, 31, 32
370101-0272A	RES, 2.7K,1/8W,5%,CF TAPE & REEL	4	R13, 33, 34, 35
370101-0472A	RES, 4.7K,1/8W,5%,CF TAPE & REEL	2	R4, 24
370101-0473A	RES, 47K,1/8W,5%,CF TAPE & REEL	1	R25
370101-05R0A	RES, 5,1/8W,5%,CF,TAPE & REEL	2	R26, 27
370101-8253A	RES, 82.5K,1/8W,5%,CF,TAPE & REEL	1	R6
370200-15R0A	RES, 15,1/4W,1%,MF,TAPE & REEL	1	R28
370202-1002A	RES, 10K,1/8W,1%,MF TAPE & REEL	1	R1
370202-1003A	RES, 100K,1/8W,1%,MF TAPE & REEL	2	R8, 22
370202-1782A	RES, 17.8K,1/8W,1%,MF TAPE & REEL	1	R20
370202-2003A	RES, 200K,1/8W,1%,MF TAPE & REEL	2	R9,21
370202-3483A	RES, 348K,1/8W,1%,MF TAPE & REEL	2	R7,23
370202-3571A	RES, 3.57K,1/8W,1%,MF TAPE & REEL	1	R2
370202-3741A	RES, 3.74K,1/8W,1%,MF TAPE & REEL	1	R3
370202-4021A	RES, 4.02K,1/8W,1%,MF TAPE & REEL	1	R17
370202-4022A	RES, 40.2K,1/8W,1%,MF TAPE & REEL	1	R18
370202-4222A	RES, 42.2K,1/8W,1%,MF TAPE & REEL	1	R5
370202-4751A	RES, 4.75K,1/8W,1%,MF TAPE & REEL	1	R10
370202-6041A	RES, 6.04K,1/8W,1%,MF TAPE & REEL	1	R36
370202-8061A	RES, 8.06K,1/8W,1%,MF TAPE & REEL (8.05K OK)	1	R16
376000-0033A	XSTR, 2N4401,NPN,GENERAL PURPOSE	2	Q1,2

Table 8-1: Parts Listing, PCBA P/N 401915-0000, CO_2 Board (3 of 3)

MDE Part Number	Description	Quantity	Reference
376000-0034A	XSTR, 2N4403,PNP,GENERAL PURPOSE	1	Q3
378000-0005A	DIO, 1N914,SIGNAL T&R	2	D5, 9
378000-0071A	DIO, 1N5258B,ZENER	1	D4
378000-0072A	DIO, BAV99,HIGH SPEED	6	D1, 2, 3, 6, 7, 8
378000-0073A	DIO, MUR110,RECTIFIER,ULTRA FAST	1	D10
384000-0189A	PRESSURE SENSOR 1210-A-015-A-3S	1	U1
401914-0000	PCB, BRICK PRYON CO2,E2B/E3B REV C (E1678)	1	-
402003-0000	HYBRID, 2300 BENCH AMPLIFIER	1	J2
402004-0000	HYBRID, 2301 ANALOG MOTOR DRIVE	1	J1
402244-0000	INDCTR, TORROID - CO2	1	L1

Table 8-2: Parts Listing, PCBA P/N 401917-0000, CO_2 Processor Board

MDE Part Number	Description	Quantity	Reference
352100-0104A	CAP, .1UF,50V,10%,RAD,X7R TAPE & REEL	2	C1, 2
354000-0317A	CONN, 5-PIN,M,DBL ROW,.1 CTR	1	J1
356000-0021A	XTAL, 16MHZ OSC IC	1	U6
364000-0028A	IC, 74HC74	1	U1
364000-0199A	S*IC, Z80180 8/10MHZ PLCC	1	U4
364000-0209A	IC, 74HC193 UP,DOWN COUNTER	1	U2
364000-0246A	S*IC,51256,SRAM,SMD,32KX8,120NS,SOP28-P-450	1	U5
364000-0278A	S*IC, 1 MEG,UNSECT FLASH PROM PLCC 32,SMD	1	U3 - NEEDS PROGRAM
365000-0168A	S*SKT, 68-PIN,LOW PROF,PLCC W/ LOCATING POSTS,SMD	1	SU4
365000-0232A	S*SKT, 32-PIN,LOW PROF,PLCC W/ LOCATING POSTS,SMD	1	SU3
370101-0101A	RES, 100,1/8W,5%,CF TAPE & REEL	1	R1
370101-0202A	RES, 2K,1/8W,5%,CF TAPE & REEL	1	R2
376000-0019A	XSTR, 2N7000,FET	1	Q1
378000-0005A	DIO, 1N914,SIGNAL T&R	1	D1
401916-0000	PCB, BRICK CO2 PROCESSOR,E2B/E3B REV C (E1600)	1	PCB1

9 Cardiac Output Board

9.1 Overview

The ESCORT II Cardiac Output system consists of a bifurcated Cardiac Output (CO) cable and the Cardiac Output board. The bifurcated CO cable is comprised of two individual cables — one with a blue connector which connects to the thermistor on the catheter to take blood temperatures, the other with a four-pin female plug which connects to an open bath temperature probe or an injectate flow through probe. The Cardiac Output board includes sensitive amplifiers, an analog-to-digital converter, digital signal processing, and voltage regulators.

The process of performing Cardiac Output measurements starts with a certain amount of injectate with a known temperature. The injectate is diluted with an unknown amount of blood inside the right ventricle of the heart. Temperatures are continuously monitored. Cardiac output, right ejection fraction (REF), stroke volume (SV), end systolic volume (ESV) and end diastolic volume (EDV) are calculated using algorithms stored inside the EPROM. The EEPROM stores the calibration coefficients for each channel. Each board has a different set of coefficients. The resistance changes on the probes are converted to voltage values with the analog amplifiers in each one of the three channels. The amplified signals are digitized by an analog-to-digital converter. The software will take these voltage values and process them through algorithms to calculate the temperature values first, and then the CO and REF values.

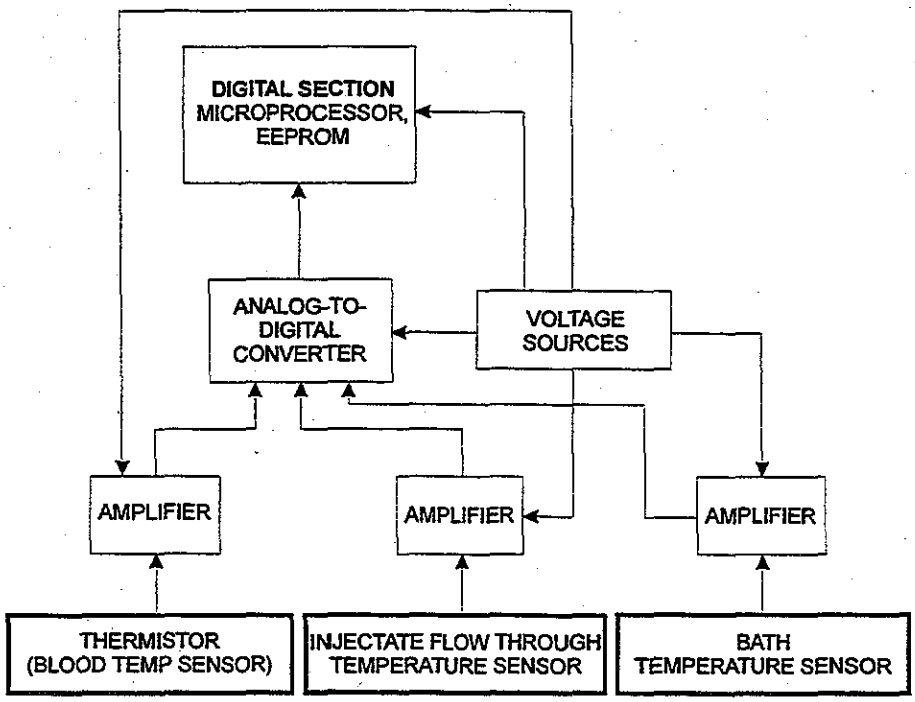


Figure 9-1: Cardiac Output Board Block Diagram

9.2 Bifurcated Cardiac Output (CO) Cable

Sensitive thermistors are mounted at the end of the catheter, the bath probe or the injectate probe. The thermistors are calibrated devices whose resistances vary in known manners with varying temperatures. The blue end of the CO cable is connected to the catheter of the CO system. The metallic connector of the CO cable is connected to a reference bath probe or an injectate sensor probe. The entire CO cable, if found to be defective, must be replaced as an assembly. The pin designations of the CO Patient Cable Connector are defined in Table 9-1.

The bifurcated cardiac output cable used with the ESCORT II is available from Baxter-Edwards, reference P/N COM-2CC.

Table 9-1: CO Patient Cable Connector

PIN NUMBER	COLOR	NAME
1	BLACK	BAB
2	BLACK	THB
3	RED	BAC
4	NOT USED	-
5	SHIELD	AI
6	NOT USED	-
7	BROWN	THD
8	RED	THA
9	ORANGE	THC
10	WHITE	BAA
11 TO 13	NOT USED	-
14	GREEN	FL

9.3 Cardiac Output Board

The CO Board may be summarized into the following sections, each section is listed below and discussed in the following text.

- Thermistor Amplifiers
- Bath Amplifier
- Flow Through or Injectate Amplifiers
- Analog-to-Digital Converter
- Microprocessor Unit
- EEPROMs and Other Memories
- Voltage Regulators

9.3.1 Thermistor Amplifiers

Thermistor signals are picked up by [THA], [THB], and [THD]. [THA] is connected to analog ground. Between the [THB] and the [THD], the resistance values changes depending on the temperature of blood samples taken inside the heart. The changes in resistances also cause changes in voltage input levels of amplifier U8B. High frequency noise is filtered out by 0.1 μF capacitors at the inputs of the operational amplifiers U8A and U8B. U8A is a voltage follower fed by -2.5 VDC. R39 and R30 provide the catheter thermistor of about -0.1 VDC. The diodes D5, D6, D7, D8, D9, D10, and D12 limit the voltage applied to the catheter to 0.7 and -1.4 VDC. R28, R25, and R24 limit the current applied to the catheter to 10 μA. Inside the catheter, a 9.76 kΩ resistor is connected between [THB] and [THA]. This resistor and the thermistor form a voltage divider. This voltage is applied to the non-inverting stage of U8B with a gain of about 1.98. R24 and C25 make a low pass filter with a cutoff frequency of about 10 Hz. The output of U8B is scaled at U4D with a 5 VDC in order to match the channel 1 input range of U5, the sigma delta analog to digital converter, which requires a signal amplitude between 0 and 5 V. U4D provides a voltage gain of about 70. The amplified output goes to the analog-to-digital converter U5-7.

9.3.2 Bath Amplifier

Bath temperatures are sensed by the temperature probe. The temperatures are converted to resistance values at [BAA], [BAB], and [BAC]. The resistance values change the voltage levels at the input of the operational amplifier U4B, which has a voltage gain of about 38. The bath probe, connected between [BAB], [BAA], and [BAC], is part of a feedback network of U8D fed by -2.5 VDC through R40. The output of U8D is scaled at U4C with -2.5 VDC in order to match the channel 3 input range of U5, the sigma delta analog to digital converter, which requires a signal amplitude between 0 and 5 V. The output of U4B goes to the analog-to-digital converter U5-9.

9.3.3 Flow Through or Injectate Amplifiers

U8C and U8D are flow through amplifiers. The flow through probe, connected between [FL] and [BAB], is part of a feedback network of U8C fed by 5 VDC through R34. The signal [FL] is connected to the flow through probe, which sends a constant current through this port and the signal [BAB]. Whenever there is a temperature change, it will cause a voltage change at the output of the U8C. The output of U8C is scaled at U4B with 5 VDC in order to match the channel 2 input range of U5, the sigma delta analog to digital converter, which requires a signal amplitude between 0 and 5 V. The signal [BAB] is connected to the bath temperature probe, which has a different constant current flowing through [BAB], [BAA], and [BAC]. A change in temperature will cause a voltage change at the output of U8D.

9.3.4 Analog-to-Digital Converter

U5 is a three-channel, gain programmable sigma delta A/D converter with bidirectional serial interface. The MODE line of the converter is tied to ground, therefore, the internal serial clock, SCLK, at U5-1 is in external clocking mode, and the SCLK line acts as an input. The signal, [SCLK_OUT], originates from the Gate Array Logic (GAL), U6. This signal contains the clocks needed to run the cardiac output acquisitions and calculations and is input to the A/D at U5-1. The master clock signal MCLKIN, at U5-2, is a 2 MHz clock pulse train, which originates from the GAL (U6-20). SYNC\ (U5-5) and STNBY\ (U5-11) are pulled up to 5 volts. DRDY\ (U5-21) is a logic output. A falling edge indicates that a new output word is available for transmission. DRDY\ will return high upon completion of transmission of a full output word. [RFS\] on U5-20, derived from U6-23, is the line for Receive Frame Synchronization. In our application, if this line goes low, the serial data output SDATA (U5-22) becomes active. [TFS\] on U5-19, derived from U6-21, is designed for Transmit Frame Synchronization. Active low logic input is used to write serial data to the device. It must go low before the first bit of the data word is written to the A/D. U5-4, the Address Input (A0), is tied to U5-19 [TFS\]. If U5-4 is low, reading and writing goes to the control register of the device. If U5-4 is high, access goes either to the data register or the calibration register of the device. U5-22 serial data, SDATA, can be either input or output. If it acts as an input, then it writes either to the control register or to the calibration register. If it acts as an output, serial data is accessed from the control register, calibration register, or the data register. During a read operation, serial data becomes active after [RFS\] goes low. During a write operation, valid serial data is expected on the rising edges of SCLK when [TFS\] is low.

The sampling rates are programmable: two channels at 12 Hz, and one channel at 24 Hz. The input range is from 0 to 5 V. The word length is 16 bits with an accuracy of 0.000644° C.

9.3.5 Microprocessor Unit

The microprocessor (U3) is a Hitachi HD64180 chip or equivalent which is pin-for-pin compatible with the Zilog Z8S180 microprocessor. It runs on an external crystal resonator of about 16 MHz at U3-3 and U3-4. It also provides an 8-MHz clock to U3-58, which is also known as CLK0. U3 pins 14 to 22 output the low-byte address lines [A0 - A7]. U3 pins 23 to 30 output the high-byte address lines [A8 - A15]. U3-31 outputs [A16], which is connected to the EPROM, U15-2. U3-32 outputs [A17], which is connected to the GAL at U6-4. U3-7, the BUSREQ\ line, and U3-5, the WAIT\ line, are tied to +5 VISO. U3 pins 37 to 44, [D0 - D7], constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles. U3-9, NMI\, the non-maskable interrupt, is tied to +5 VISO. U3-10, [TIMETIKI], is the maskable interrupt request 0, which provides the time base for software synchronization. This signal comes from the main CPU board of the ESCORT II. The processor acknowledges this interrupt request with an interrupt acknowledge cycle. U3-11, INT1\, the maskable interrupt request 1, is tied to +5 VISO. U3-12, INT2\, the maskable interrupt request 2, is connected to the analog-to-digital converter U5-9, DRDY\. U3-67, RD\ (the read line), is connected to the Flash EPROM, U15-24, the SRAM, U7-22, and the 8K x 8-bit EEPROM, U14-22. Depending on the address selected, the microprocessor may get data from any one of these memory devices. U3-66, WR\ (the write line), is generated by the GAL U6-27. It is connected to the Flash EPROM, U15-31, the 32K SRAM U7-27, and the 8K x 8 bit EEPROM, U14-27. U3-63, [ME\], the memory enable line, is connected to U6-13. It is low when active. U3-52, [IOE\], the input/output enable line, is connected to U6-6. It is also low when active. U3-8, [RST1], is generated by U13-6, which in turn is controlled by [RESETI\], generated from the mother board CPU. U3-51, [TXD], transmit data 1, outputs ASCI channel data to P2 header pin 1. Transmitted data changes are with respect to the falling edges of the transmit clock. U3-54, [CKA1], is the transmit and receive clock for the synchronous channel. U3-48, [CPU_RXI], outputs data to the motherboard CPU from the ASCI channel of the processor, and it is connected to P1 cardedge pin 15. U3-49, [CPU_TX1], receives data from the motherboard CPU, and is connected to P1 cardedge pin 17.

The [CPU_TX1] and [CPU_RX1] signals are serial communications signals (Dbus Interface) between the CO parameter and the main CPU board of the ESCORT II monitor.

9.3.6 EEPROMs and Other Memories

The CO board contains a 128K Flash EPROM (U15), an 8K x 8 bit EEPROM (U14), a 32K static RAM (U7), and an GAL 6001 (U6) for dedicated cardiac output algorithms and calibration coefficients. The Flash EPROM contains data from address locations 00000 to 1FFFF hexadecimal, while the SRAM takes in data from address locations 20000 to 27FFF hexadecimal. Under program control, these memory devices supply data to the motherboard CPU and deliver proper information to the ESCORT II display screen.

9.3.7 Voltage Regulators

+15VISO is delivered by the P1 cardedge pins 23, 24 and 25. The +15 VDC line is connected to the voltage regulator U12 input. The voltage is regulated to +8 VDC, which is further regulated down to +5 VDC by U10. -15VISO is also delivered by the P1 cardedge pins 21 and 22. The -15VDC is connected to the negative regulator U9 input, which is regulated down to -5 VDC. The -5 VDC, together with the +5 VDC from U1 is divided down to -2.5 VDC by U4A. The -2.5 VDC supplies the inputs to U8A and U8D.

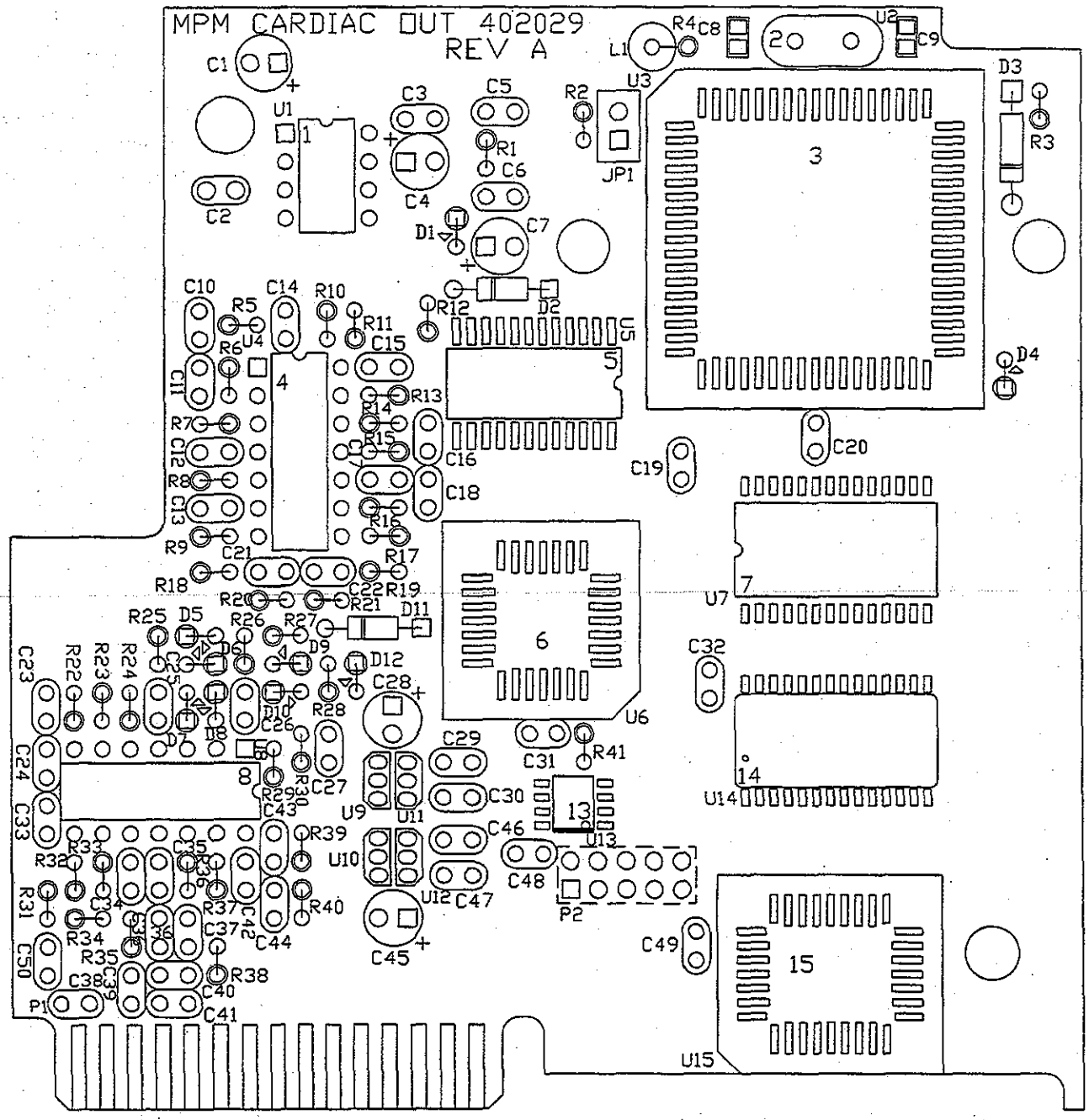


Figure 9-2: CO Board Layout